CMPE 640: Principles of VLSI Design
Lab Cover Page

Lab # : Final Project Submission
Lab Title : VHDL Code & Layout for 64byte cache

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TA / Grader Use Only:

Late Submission Deduction (20% per day late):

Other Deductions:

Final Lab Grade:

Comments to student:

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Part 1: Cache Design

In the simplified CPU memory hierarchy diagram, the position of the cache after the CPU registers, which are running at the CPU clock speed. However, CPU registers are very small in number, hence it needs other memory to perform the task. The second component of the memory hierarchy is cache, which is very fast. For example, in case of read hit means if the cpu wants a date which is present in the cache, it needs only two clock cycles to get the data. Typically, Static random access memory (SRAMs) are used to build the cache memory and there are different levels of cache as well such as L1 or level 1, L2 or level2 and L3 or level 3.

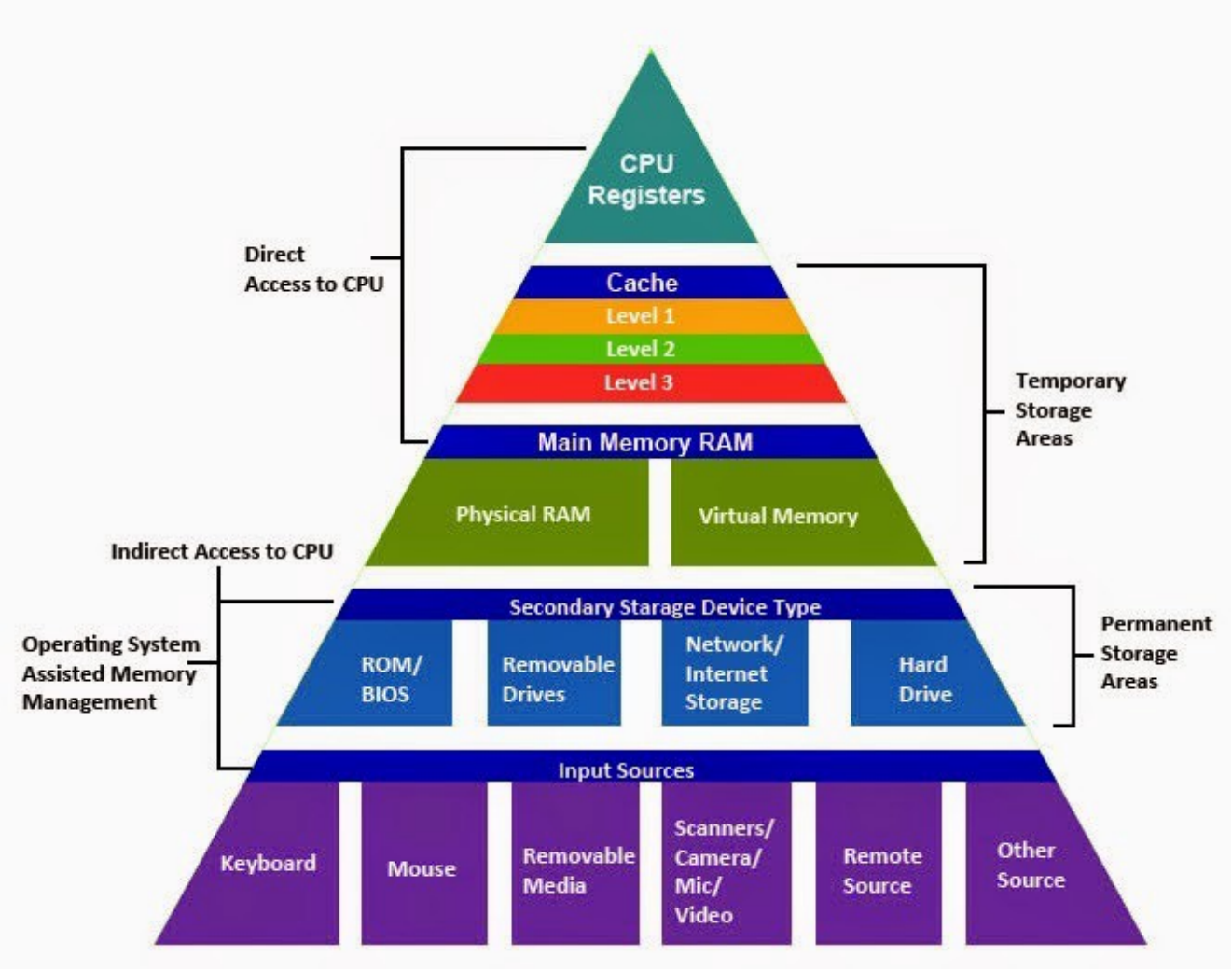


Fig1: Simplified Computer memory hierarchy

Input-output to the cache chip

In my cache design, I didn't use the typical SRAM block to design the cache. Rather I have used the positive level sensitive D-latch with transmission gate for simplicity. My 64byte cache is composed of two 32 byte cache, which has 8 blocks and each block has 4 bytes. Hence, I need 3 bits to select one of the 8 blocks and 2 bits to select the correct byte from the block. However, the remaining 3 bits from the 8 bit address are used as a tag. Tag is used to match whether the data is present in the cache or not. There is one more bit named as valid bit is used in the cache to determine whether the block of the cache is valid or not.

The start signal from the CPU marks the beginning of an operation.

The input and output of the cache blocks are

- CPU address which is 8 bit. Address will be provided by the CPU on the rising edge of the clock along with the start signal although the Cache is negative edge triggered.
- CPU data which is also 8 bit, this data bus serves two purposes such as it provides CPU data for write operation and takes cache data for read operation. Like address, the data will also be provided by the CPU on the rising edge of the clock along with the start signal although the Cache is negative edge triggered.
- 1 bit read_write signal is also provided by the CPU. If the signal is high CPU is requesting a read operation, if low a write operation.
- A 1 bit start signal is provided by the CPU at the beginning of any task performed by the CPU. This is a handshaking signal indicating the start of a read/write request from the CPU, goes high on a positive edge although my cache chip works on the negative edge.
- Another 1 bit signal named as reset acts as a master reset to the chip. A high on reset should invalidate all the entries in the cache and reset your state machine to its reset state.
- There is a Clock signal to the cache chip provided by the CPU in order to perform synchronous performance.
- Since my cache is a direct memory mapped cache, in case of the miss operation, it needs to populate the data from the memory address. It is to be noted that the memory will send the data for all the blocks so the last two bit of the memory address will always be zero.
- After any miss operation, cache will receive the data from the memory. It takes the memory 8 clock cycles after getting the enable signal to provide the first byte of data. It will sequentially provide four bytes of data required for the whole block. The first data byte will become valid on the 8th negative edge after asserting enable and will stay stable for 2 clock cycles. The next byte will be provided on the 10th negative edge after asserting enable and will stay stable for 2 clock cycles. The last two data bytes will have similar timing and will be provided on the 12th and 14th negative edges.
- There is also a memory enable signal to enable the memory at the beginning of the miss operation.
- A 1 bit busy signal is used for the handshaking operation indicating to the CPU that the cache chip is processing the previous request.

Basic operation of the cache chip

There are mainly four basic types of operation performed by the cache namely-Read Hit, Read Miss, Write Hit, Write Miss, which are described as follows.

Read Hit operation

For Read hit operation, the valid block should be enabled and the tag cache should be matched with the tag address from the CPU. For example, in the following table:

		Bytes - cache 0				Block address
valid	tag	11	1O	O1	OO	
1	111	OO	12	34	FF	000
0						001
0						010
1	1O1	56	BB	CC	DD	011
1						100
1	110	11	22	99	44	101
0						110
1	111	CC	55	67	AB	111

If the CPU address is 110-101-00 means the tag-110, block-101, and byte-00; this tag is matched with the present tag for the block-101 of the cache. Hence, this is a read- hit operation. And the data **44** will be sent to the CPU.

Read miss operation

For Read hit operation, the valid block may not be enabled and the tag cache will not match with the tag address from the CPU. For example, in the following table:

		Bytes - cache 0				Block address
valid	tag	11	1O	O1	OO	
1	111	OO	12	34	FF	000
0						001
0						010
1	1O1	56	BB	CC	DD	011
1						100
1	110	11	22	99	44	101
0						110
1	111	CC	55	67	AB	111

If the CPU address is 100-101-01 means the tag-100, block-101, and byte-01; this tag is not matched with the present tag for the block-101 of the cache which is 110. Hence, this is a read-miss operation. In case of this operation, we need to populate the cache directly from the memory and then send the data to the CPU. For that, the cache will send the address 100-101-00, since it will take the whole block, although the byte address provided by CPU is 01. Say, the data present that address in the memory is 88-99-33-44.

		Bytes - cache 0				Block address
valid	tag	11	1O	O1	OO	
1	111	OO	12	34	FF	000
0						001
0						010
1	11O	56	BB	CC	DD	011
1						100
1	**100**	**88**	**99**	**33**	**44**	101
0						110

1	111	CC	55	67	AB	111

And the data **44** will be sent to the CPU.

Write Hit operation

For Write hit operation, the valid block should be enabled and the tag cache should be matched with the tag address from the CPU. For example, in the following table:

		Bytes - cache 0				Block address
valid	tag	11	1O	O1	OO	
1	111	OO	12	34	FF	000
0						001
0						010
1	1O1	**06**	BB	CC	DD	011
1						100
1	110	11	22	99	44	101
0						110
1	111	CC	55	67	AB	111

If the CPU address is 101-011-11 means the tag-101, block-011, and byte-11; this tag is matched with the present tag for the block-011 of the cache. Hence, this is a write- hit operation. Now, if the data provided by the CPU is 06, this value will be written on the byte-11, and the present value 56 will be replaced by the 06.

Write Miss operation

For Write Miss operation, the valid block may not be enabled and the tag cache will not match with the tag address from the CPU. For example, in the following table:

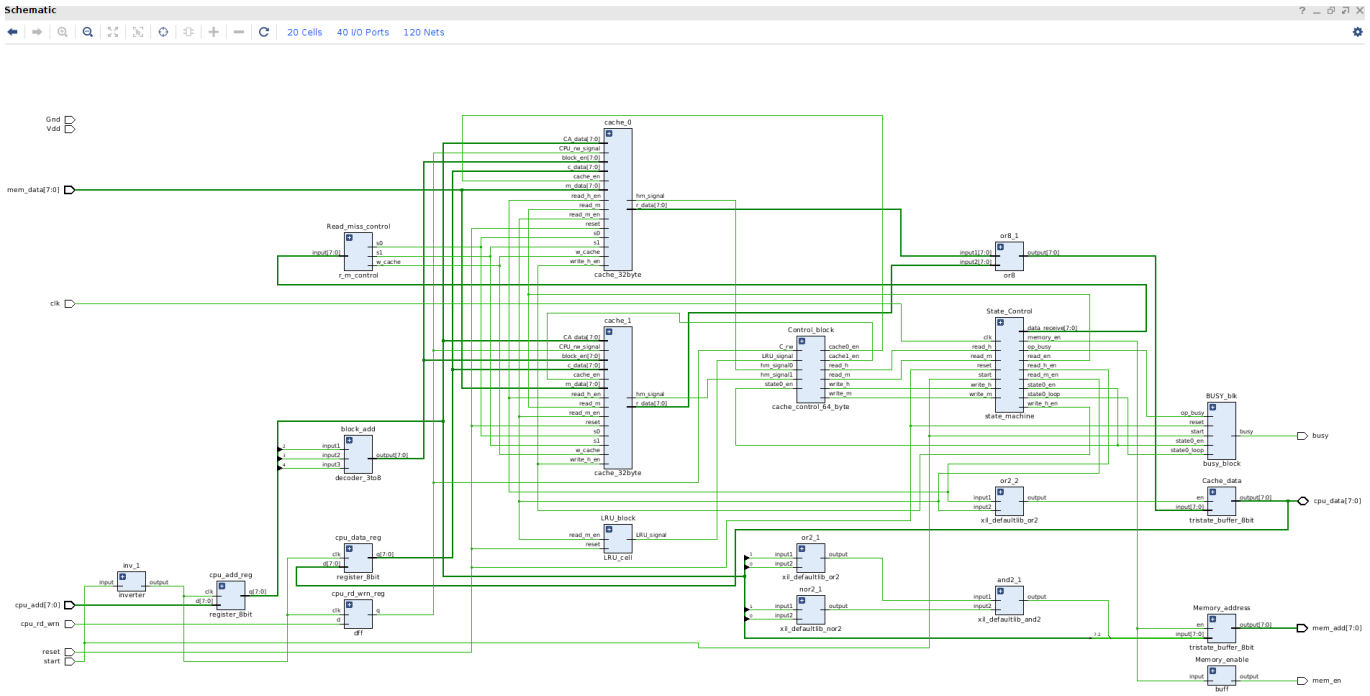
		Bytes - cache 0				Block address
valid	tag	11	1O	O1	OO	
1	111	OO	12	34	FF	000

0						001
0						010
1	1O1	**06**	BB	CC	DD	011
1						100
1	110	11	22	99	44	101
0						110
1	111	CC	55	67	AB	111

If the CPU address is 101-100-11 means the tag-101, block-100, and byte-11; this tag is not matched with the present tag for the block-100 of the cache. Hence, this is a write- miss operation. And we will not perform anything, since this is a very difficult task and for our project, we will not do anything, just a no operation.

Hierarchy of Cache

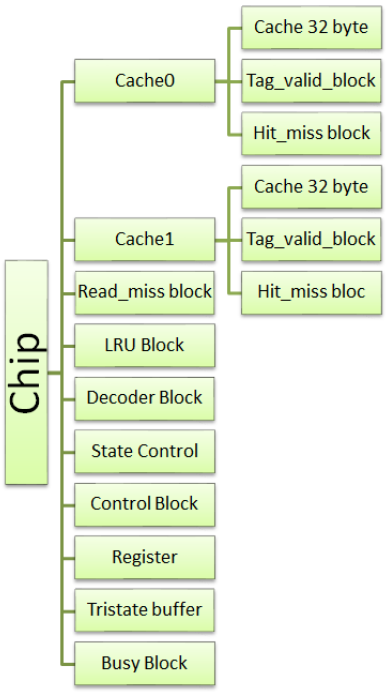
In this project, I have adopted the hierarchical structure for designing the cache as shown the following in figure.



The top-level schematic is titled as chip which consists of

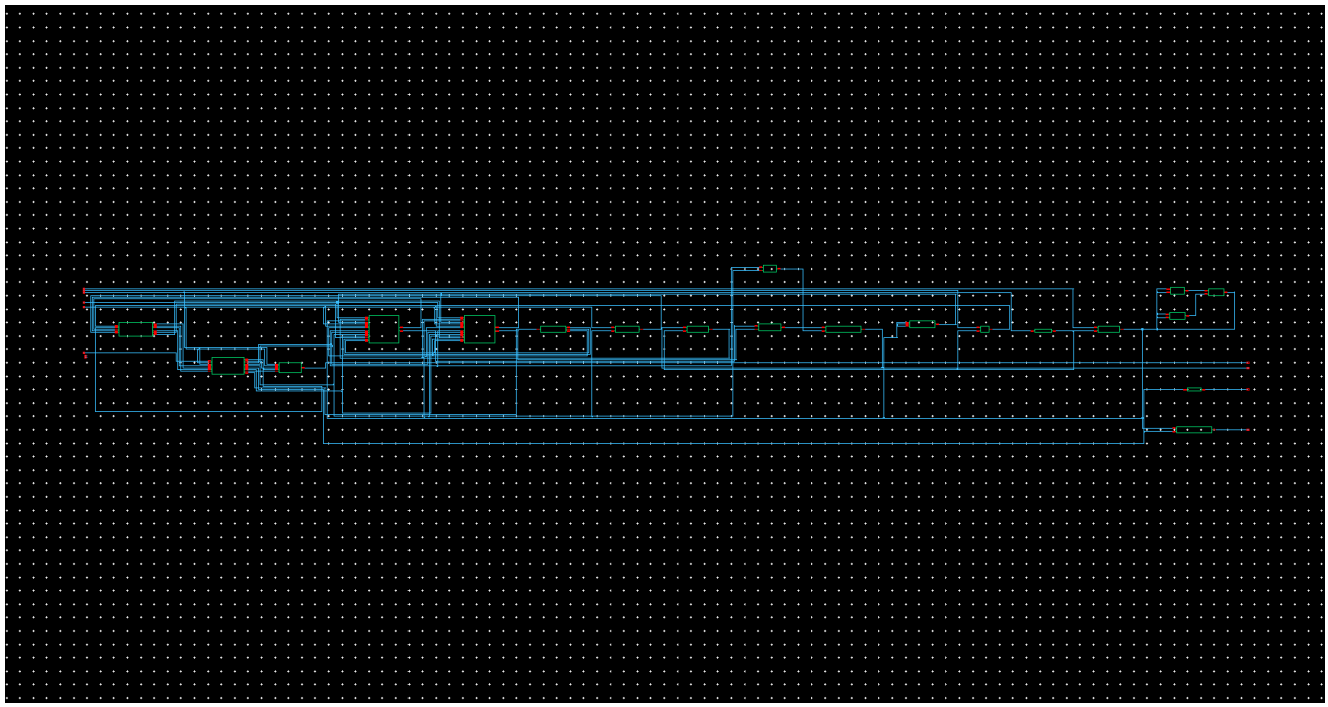
- Cache_32 byte
- Read_miss_control
- Decorder_block
- 8 bit register block
- LRU block
- Control block
- State control block
- Busy block,
- Tristate_buffer, and
- Some primitive cells

Design Hierarchy:

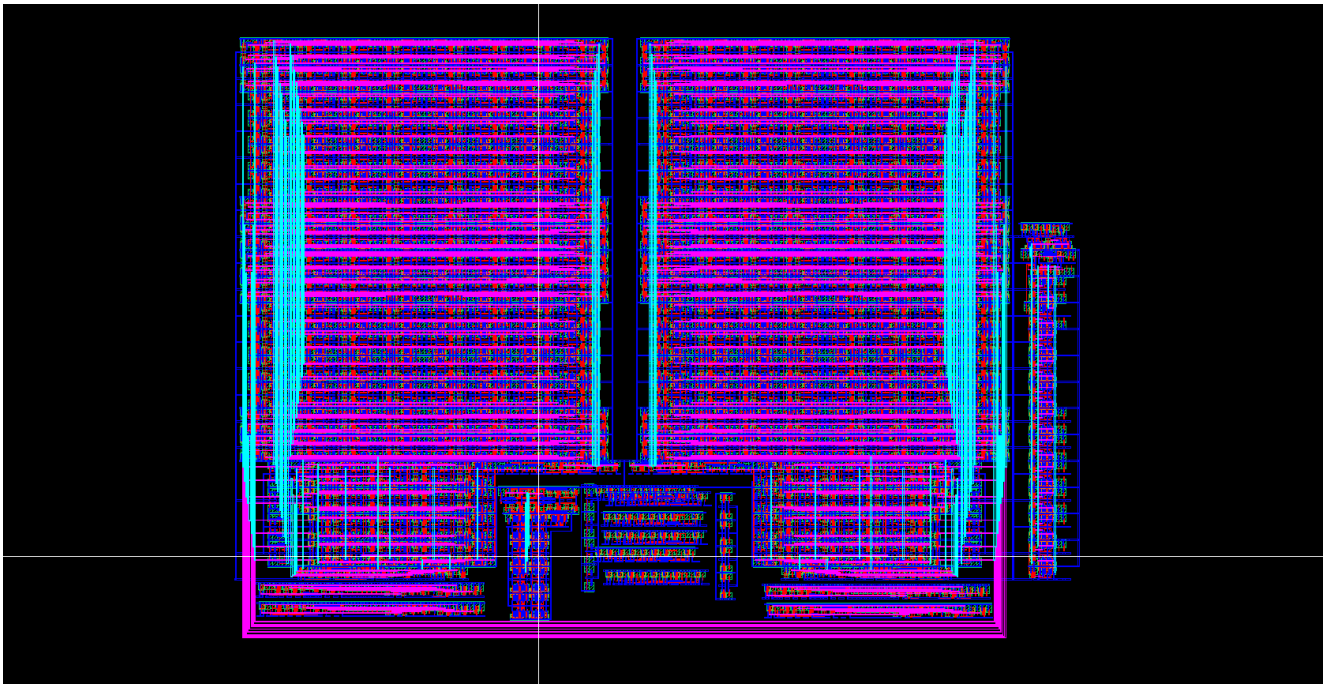


All the blocks in the top-level hierarchy are described in the following section.

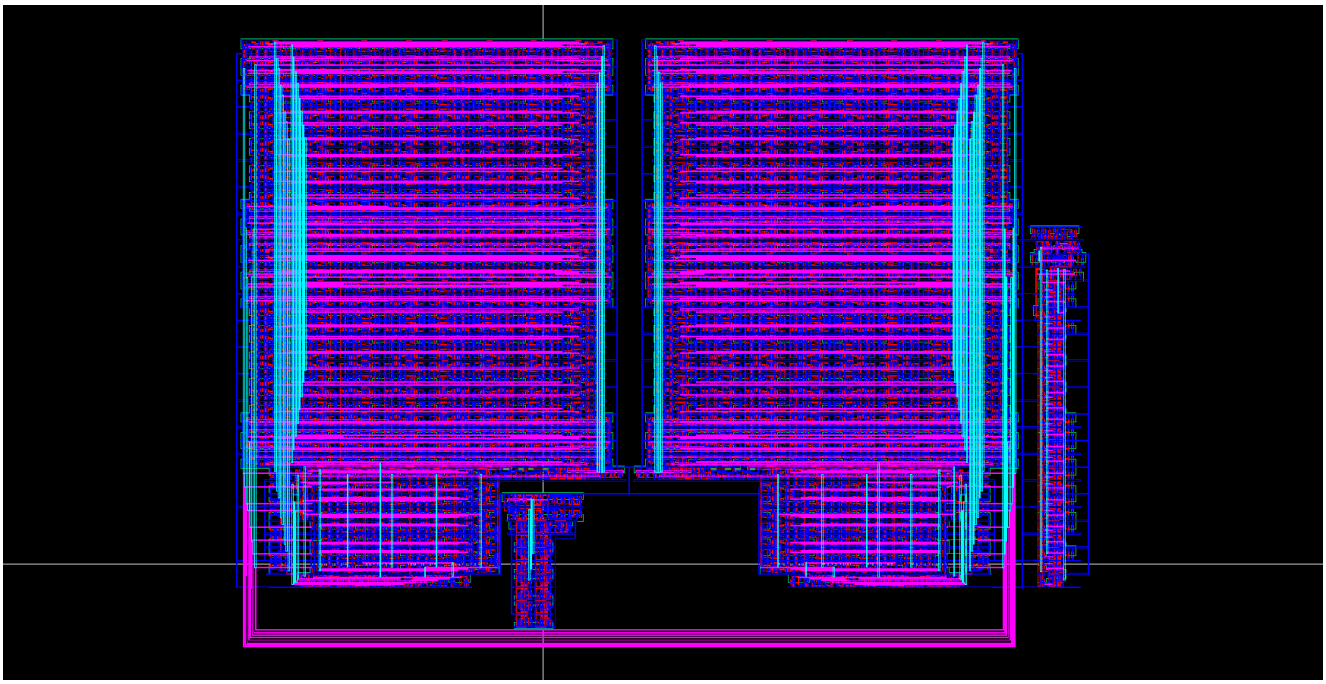
Chip Schematic diagram:



Chip layout diagram:



Chip extracted:

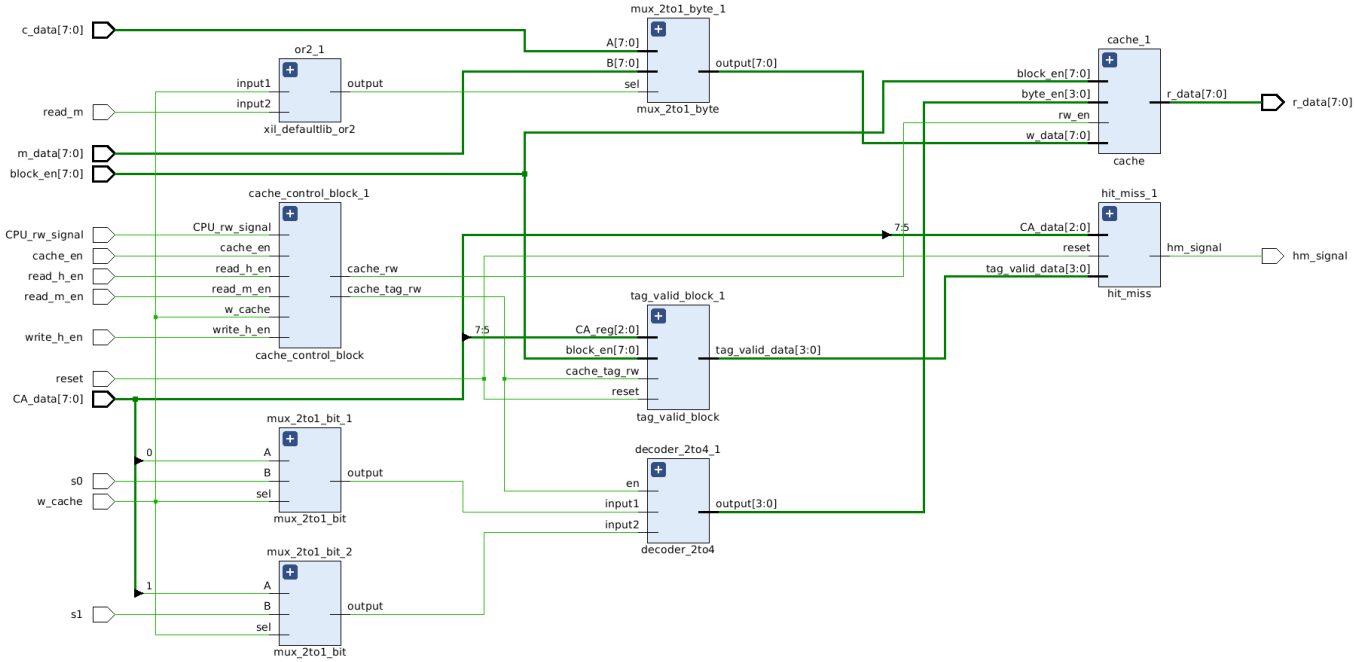


Part 2: Design of Cache_32byte_block

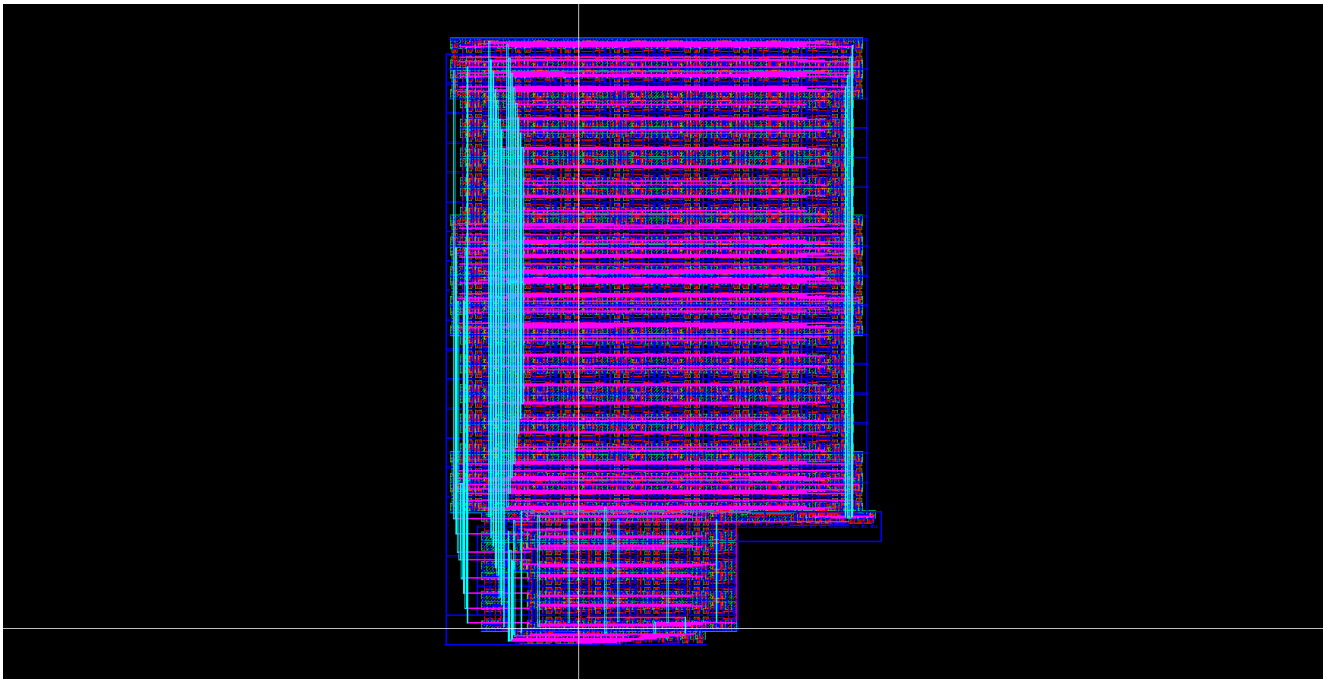
The cache_32_byte_block is mainly consist of

- Cache_block
- Cache_control_block
- Tag_valid block
- Hit_miss block
- Decoder_2to4 block
- Mux_2to1_bit block
- And some primitive cells as illustrated in the following figure.

The cache 32_byte block mainly takes CPU_data, memory_data, block_enable, CPU_rw signal, reset, CPU_address, reset, etc as the input and produces read_data and hit_miss signal as an output.


c_data[7:0]
read_m
m_data[7:0]
block_en[7:0]
CPU_rw_signal
cache_en
read_h_en
read_m_en
write_h_en
reset
CA_data[7:0]
s0
w_cache
s1
or2_1
input1
input2
output
xil_defaultlib_or2
mux_2to1_byte_1
A[7:0]
B[7:0]
sel
output[7:0]
mux_2to1_byte
cache_control_block_1
CPU_rw_signal
cache_en
read_h_en
read_m_en
w_cache
write_h_en
cache_rw
cache_tag_rw
cache_control_block
mux_2to1_bit_1
A
B
sel
output
mux_2to1_bit
mux_2to1_bit_2
A
B
sel
output
mux_2to1_bit
0
1
7:5
tag_valid_block_1
CA_reg[2:0]
block_en[7:0]
cache_tag_rw
reset
tag_valid_data[3:0]
tag_valid_block
decoder_2to4_1
en
input1
input2
output[3:0]
decoder_2to4
cache_1
block_en[7:0]
byte_en[3:0]
rw_en
w_data[7:0]
r_data[7:0]
cache
r_data[7:0]
hit_miss_1
CA_data[2:0]
reset
tag_valid_data[3:0]
hit_miss
hm_signal
hm_signal

Layout of 32byte cache



Cache_block:

The cache_block is mainly consisted of

- Cache Block_cell, which is consisted of
    - Cache byte_cell, which is consisted of
        - Cache_bit_cell, which is consisted of
            - D_latch
            - And_gate
            - Tri_state_buffer
                - T_x gate

The inputs of the Cache are block enable, byte enable, read_write signal, and the write data. And the output will be the read data.

The basic cells are shown in the following figure.

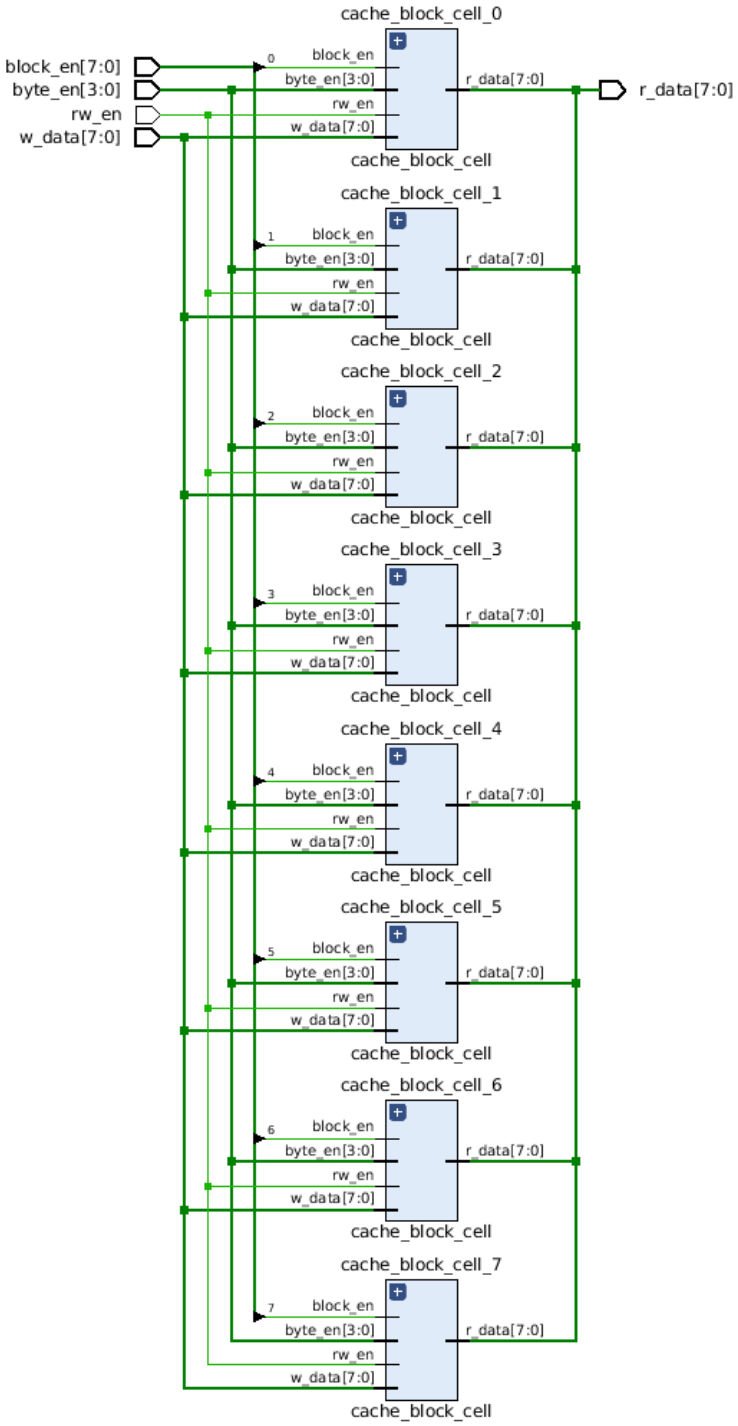
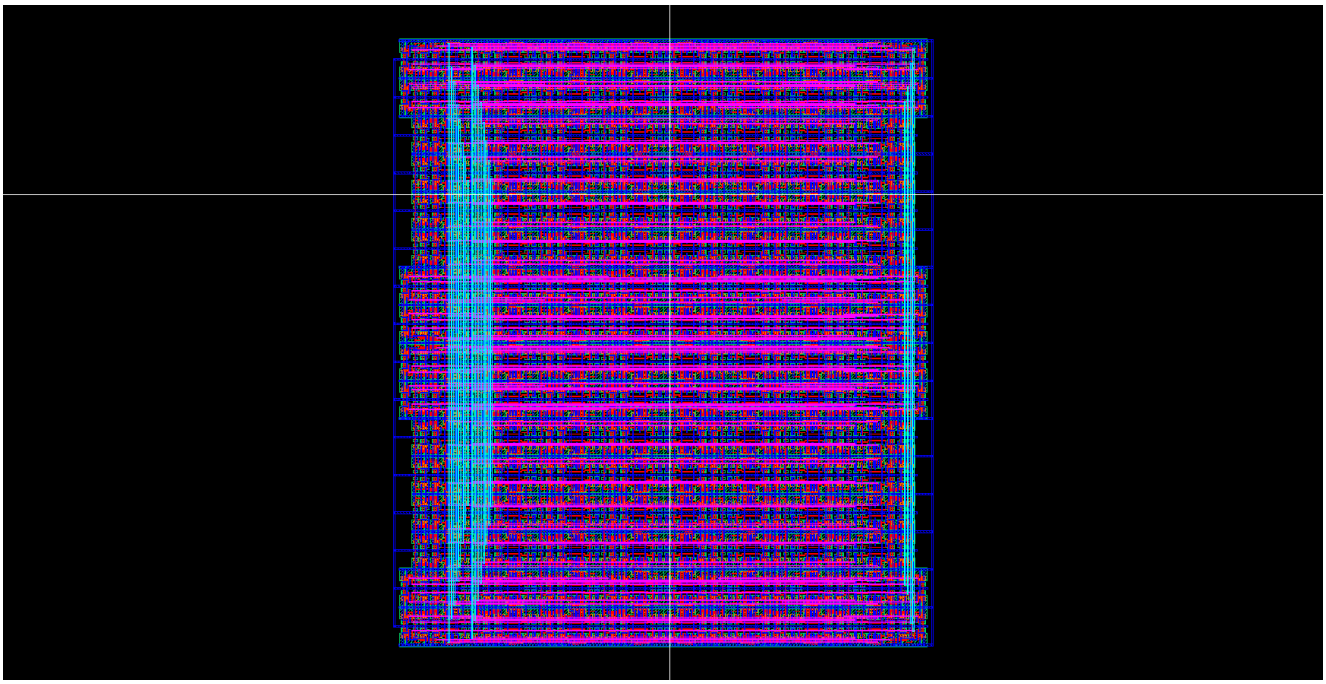


Figure : Cache

Layout of cache



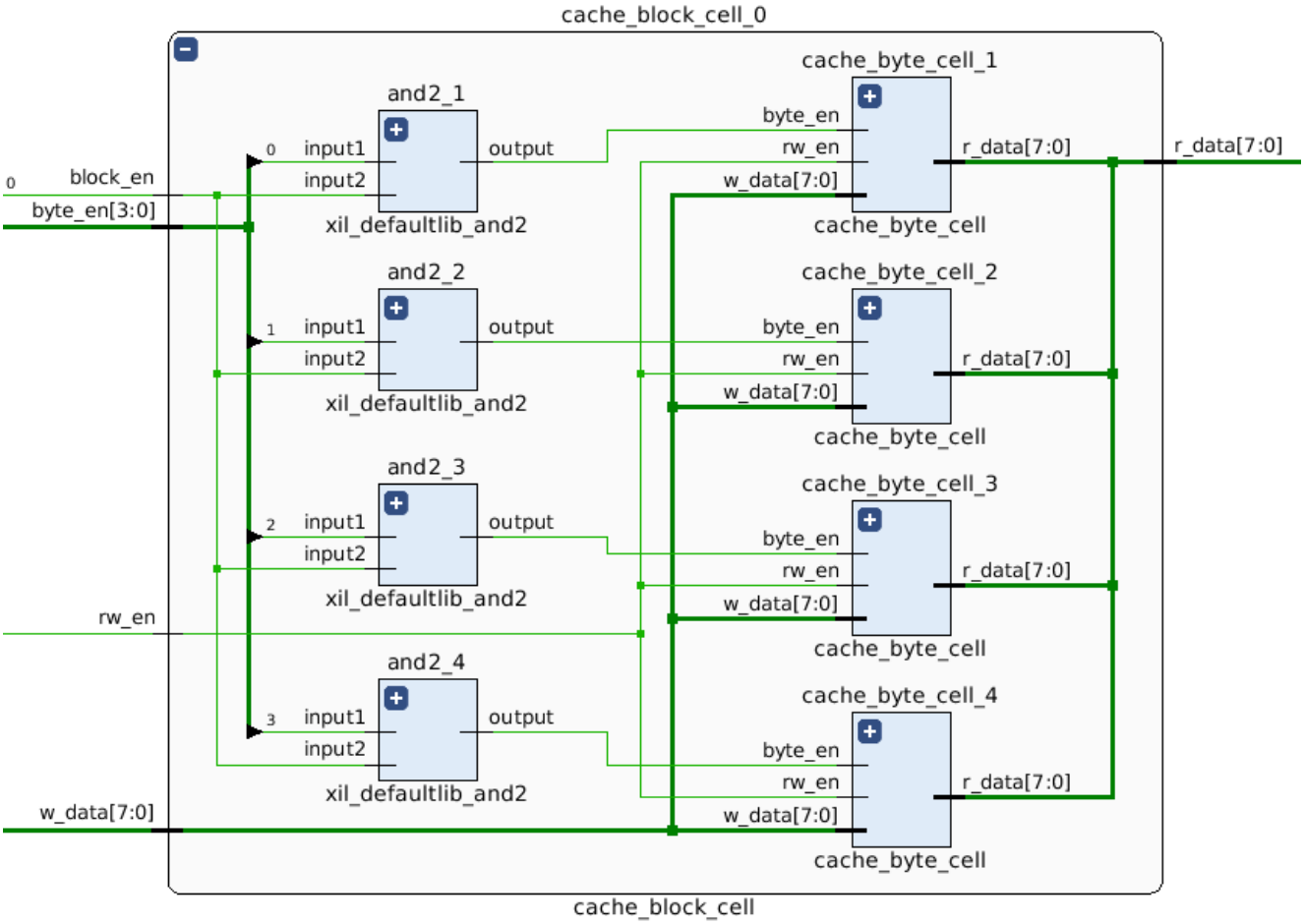
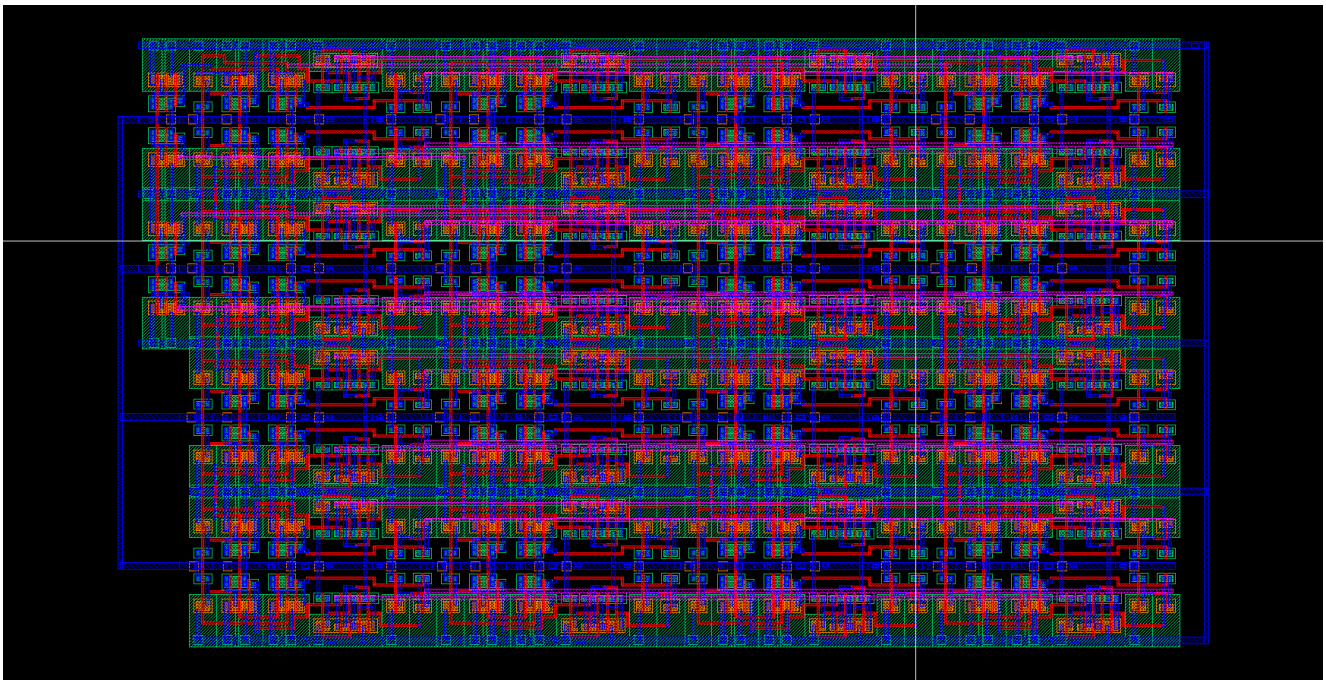
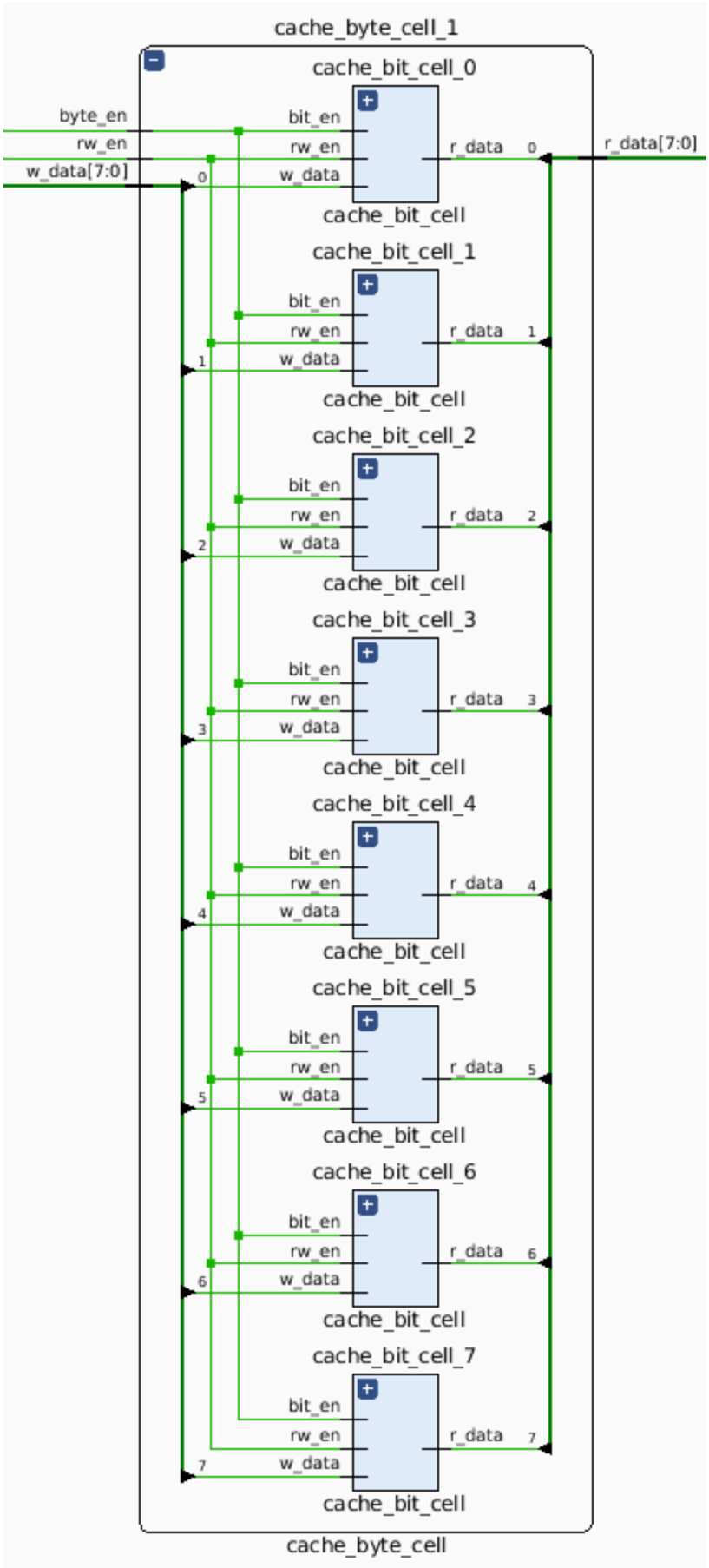


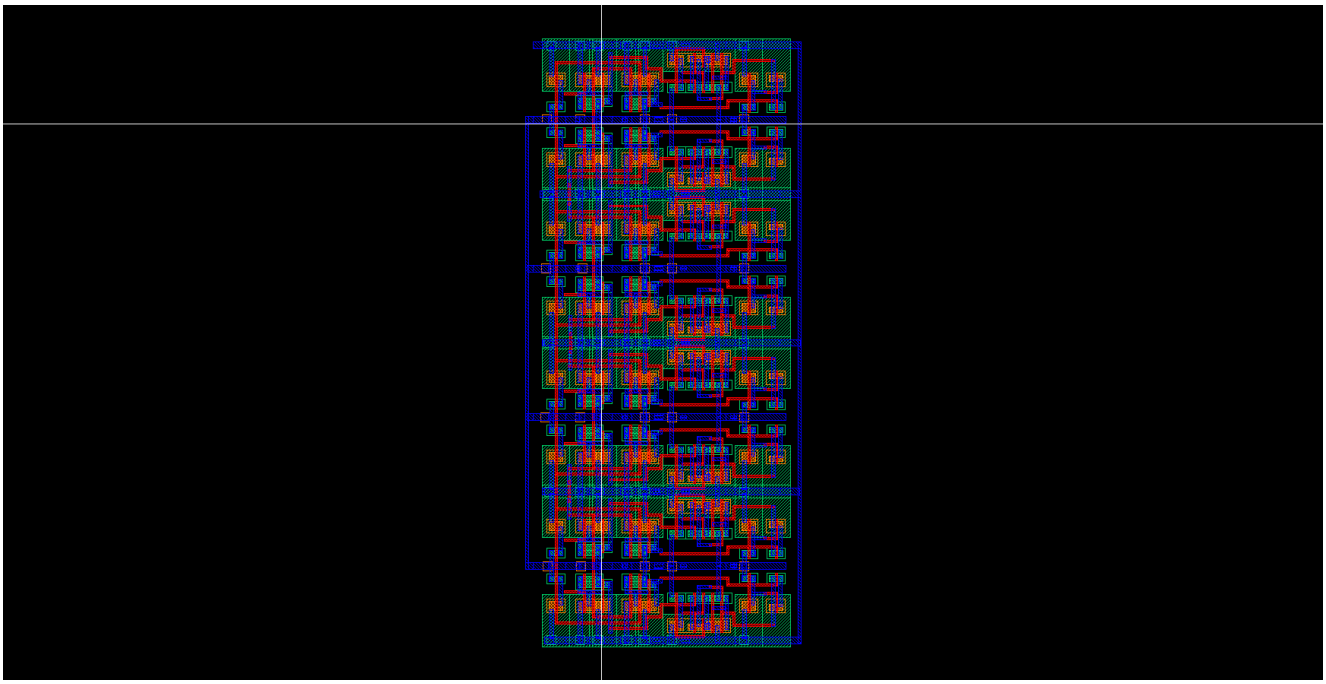
Figure : Cache_block_cell

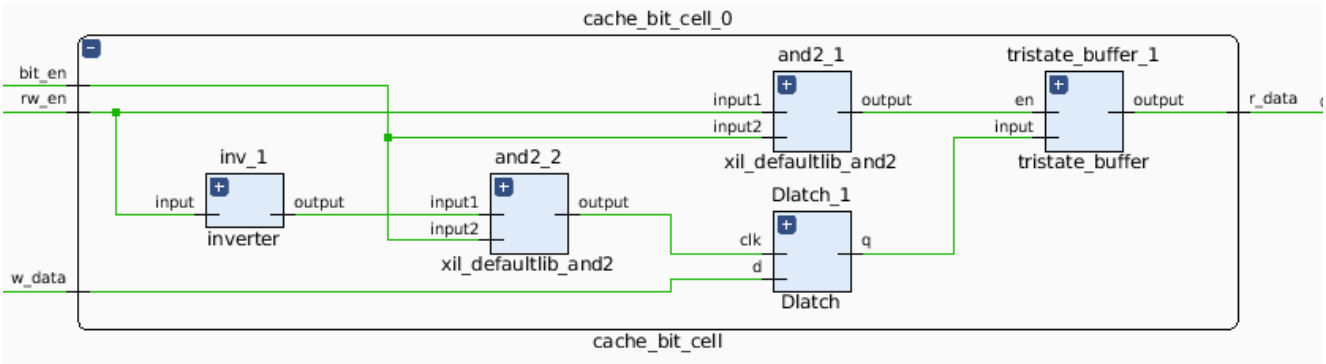
Layout of cache-block cell



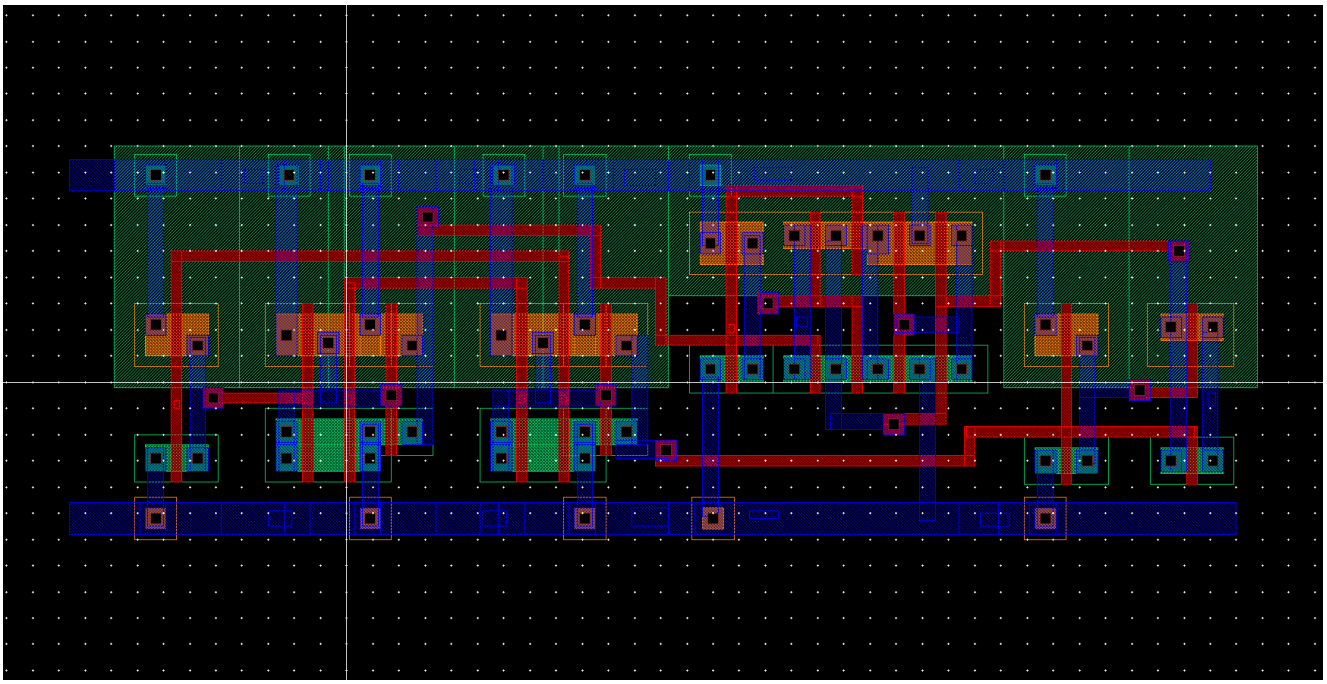

cache_byte_cell_1
cache_bit_cell_0
byte_en
rw_en
w_data[7:0]
bit_en
rw_en
w_data
r_data
0
r_data[7:0]
cache_bit_cell
cache_bit_cell_1
1
cache_bit_cell
cache_bit_cell_2
2
cache_bit_cell
cache_bit_cell_3
3
cache_bit_cell
cache_bit_cell_4
4
cache_bit_cell
cache_bit_cell_5
5
cache_bit_cell
cache_bit_cell_6
6
cache_bit_cell
cache_bit_cell_7
7
cache_bit_cell
cache_byte_cell

Layout of cache-byte cell





Layout of cache-bit cell

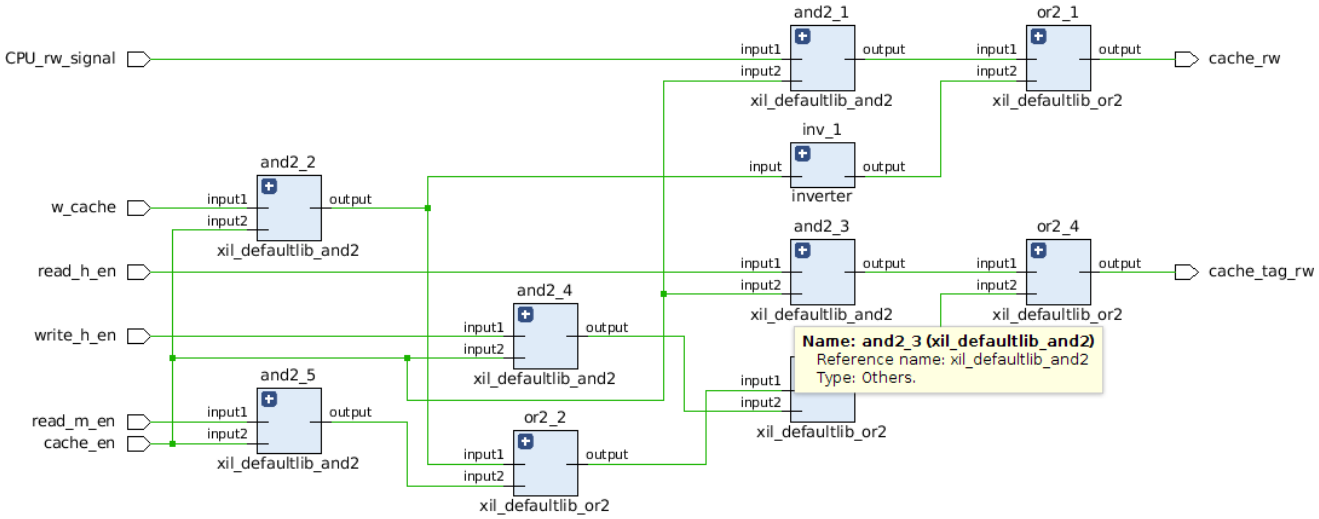


Cache_control_block

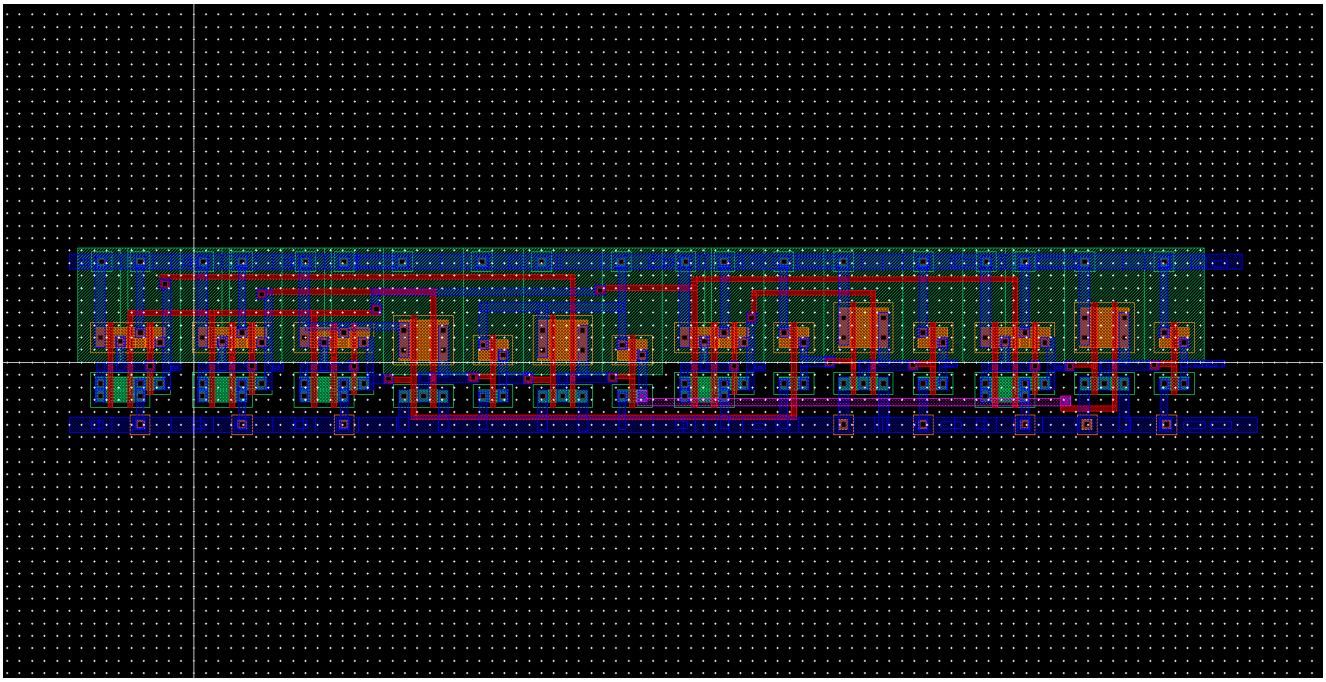
Cache control block is the building block to control the read and write operations based on the read_hit, write_hit, read_miss, and write miss signal. The cache only allows read/write depending on the output cache_rw and cache_tag_rw.

For hit operation, we don’t need to write tags.
However, for missed operations, we need to write a tag.

The cache control blocks are based on the primitive logic cells such as and, or, an inverter as shown in the following figure.

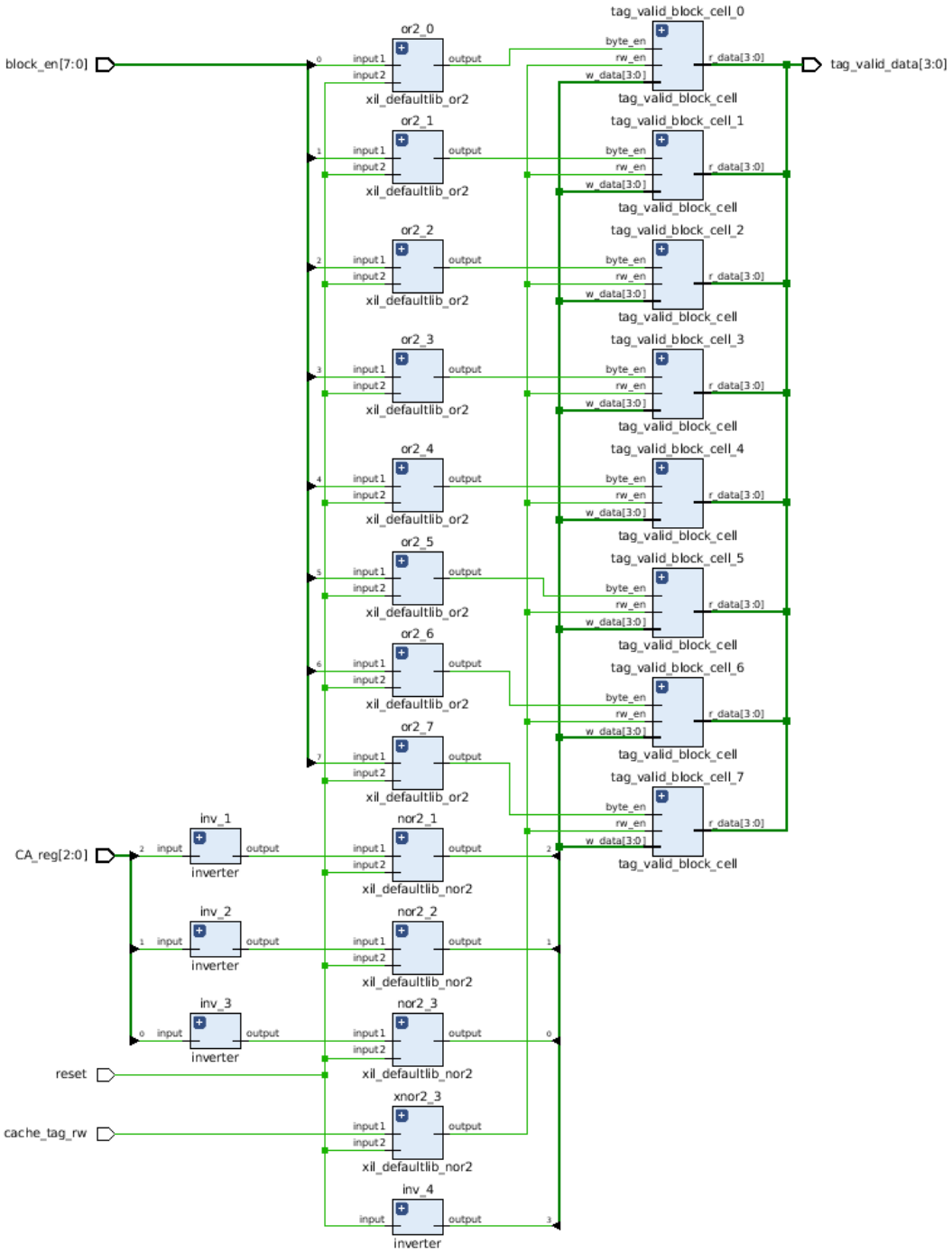


Layout of Cache_control_block

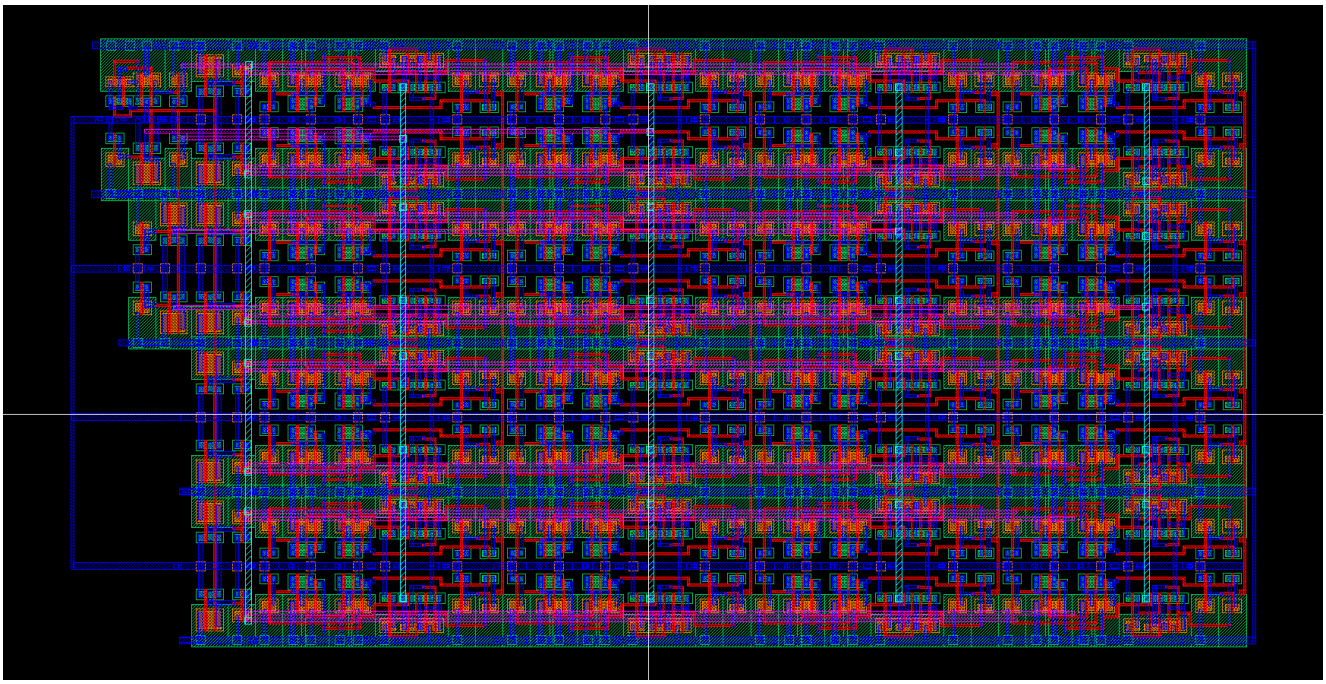


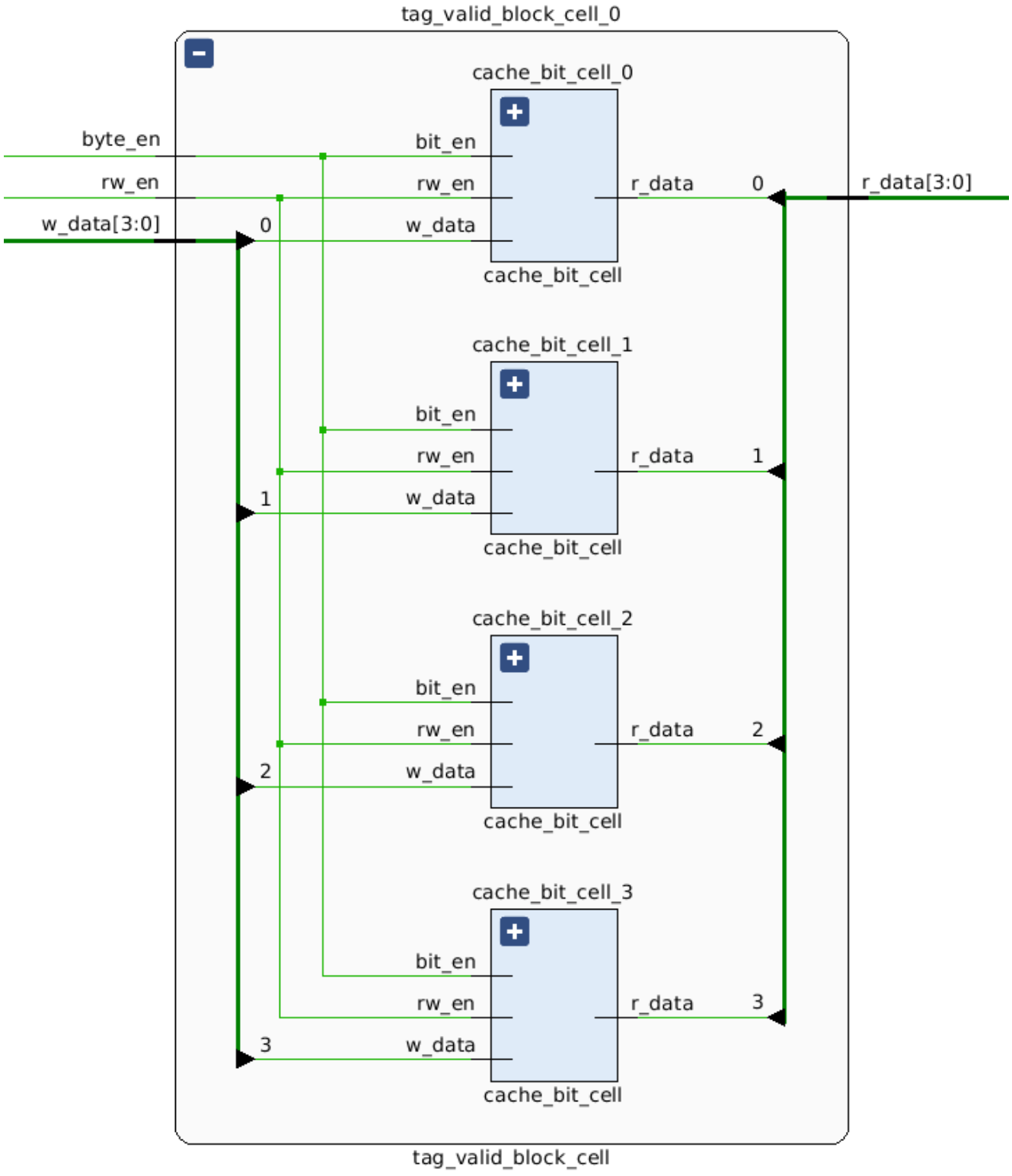
Tag_valid block

The tag_valid block, which determines whether the tag is valid or not. It has some primitive logic gate to enable the reset function, since the valid bit will be reset after the reset signal. The input here is the block enable, which means which block is needed and then the cpu address. The diagram is shown as belows

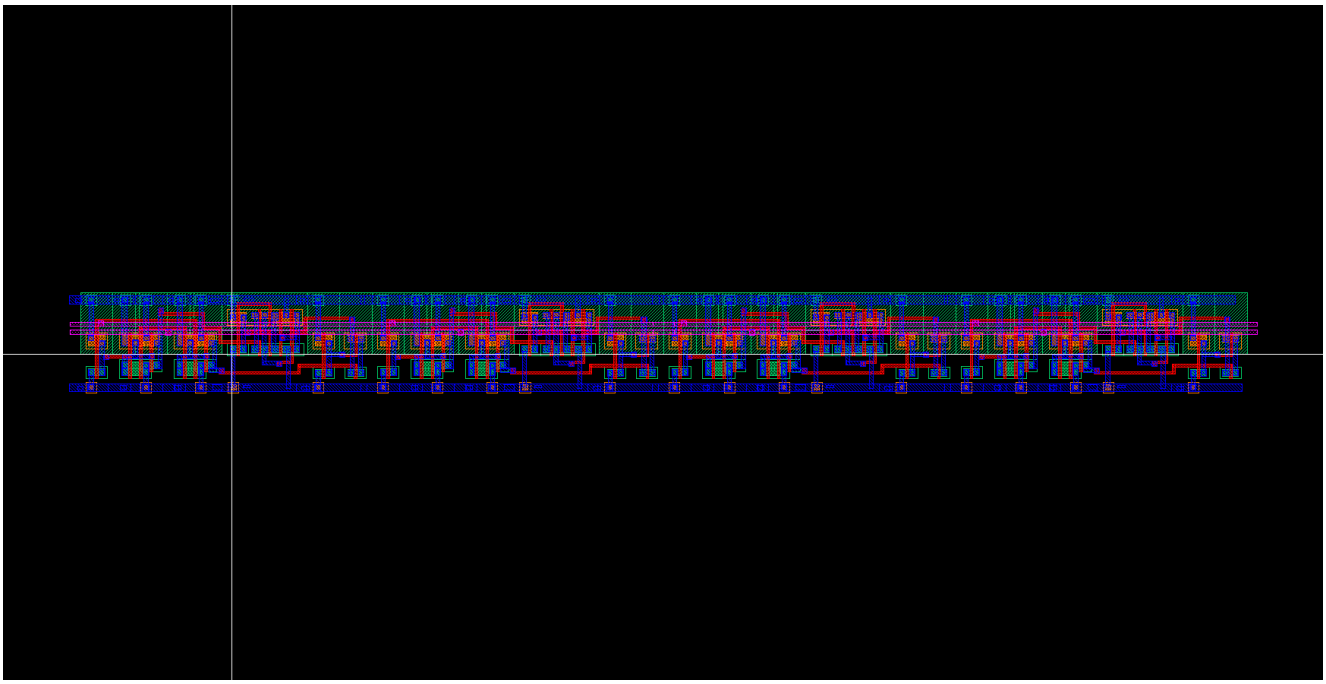


Layout of Tag_valid block



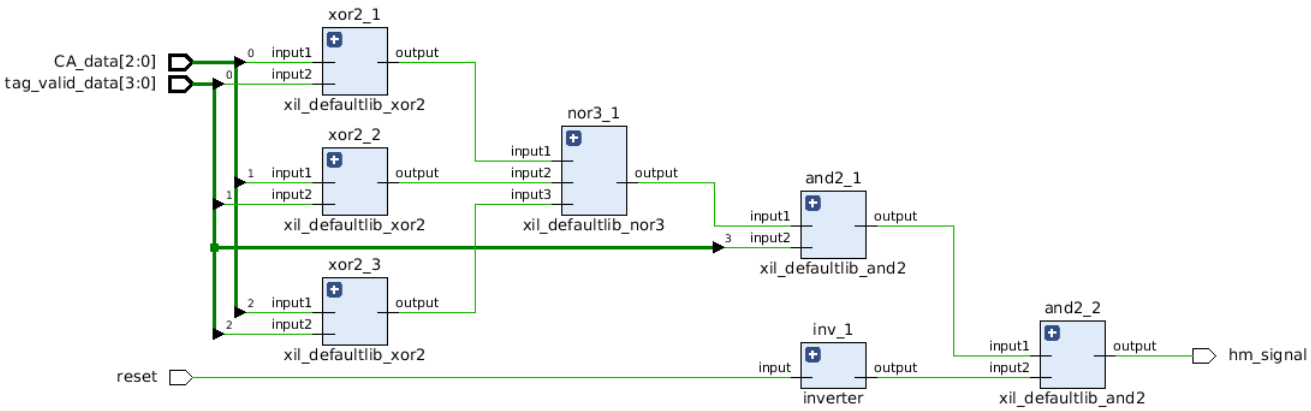

tag_valid_block_cell_0
cache_bit_cell_0
byte_en
rw_en
w_data[3:0]
bit_en
rw_en
w_data
r_data
0
r_data[3:0]
cache_bit_cell
cache_bit_cell_1
bit_en
rw_en
w_data
r_data
1
1
cache_bit_cell
cache_bit_cell_2
bit_en
rw_en
w_data
r_data
2
2
cache_bit_cell
cache_bit_cell_3
bit_en
rw_en
w_data
r_data
3
3
cache_bit_cell
tag_valid_block_cell

Layout of Tag_valid block-bit cell

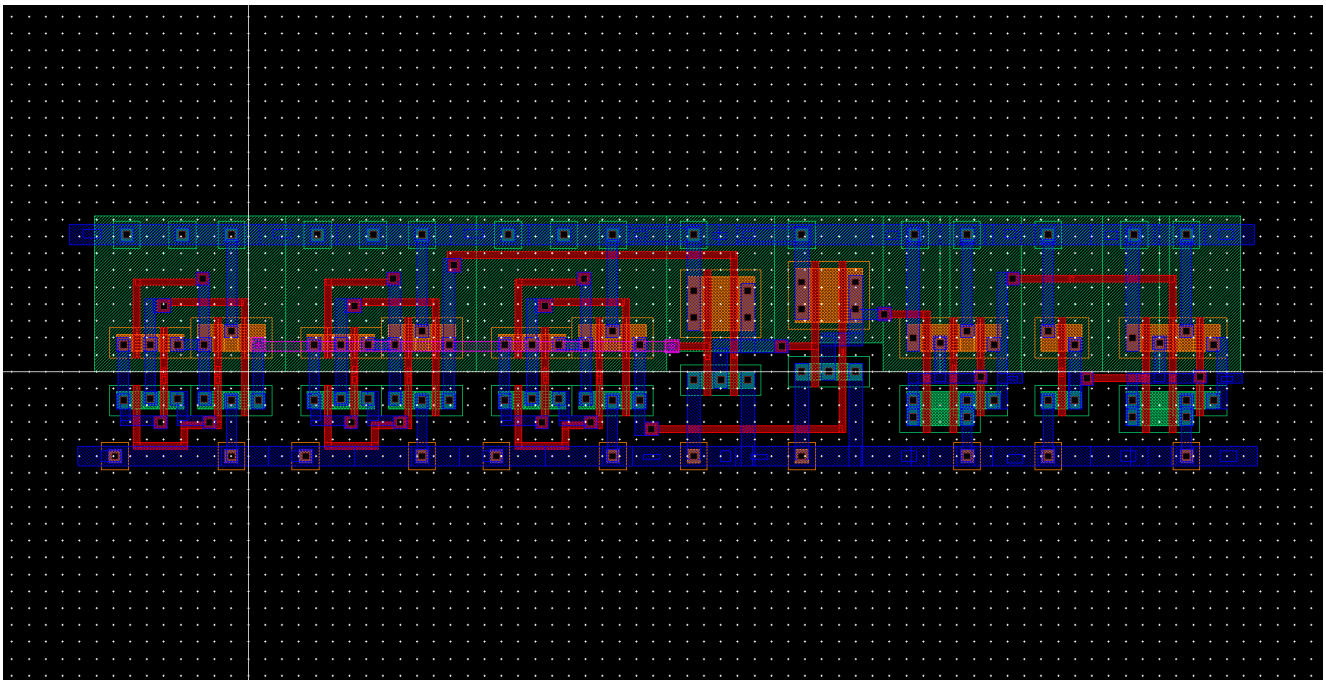


Hit_miss block

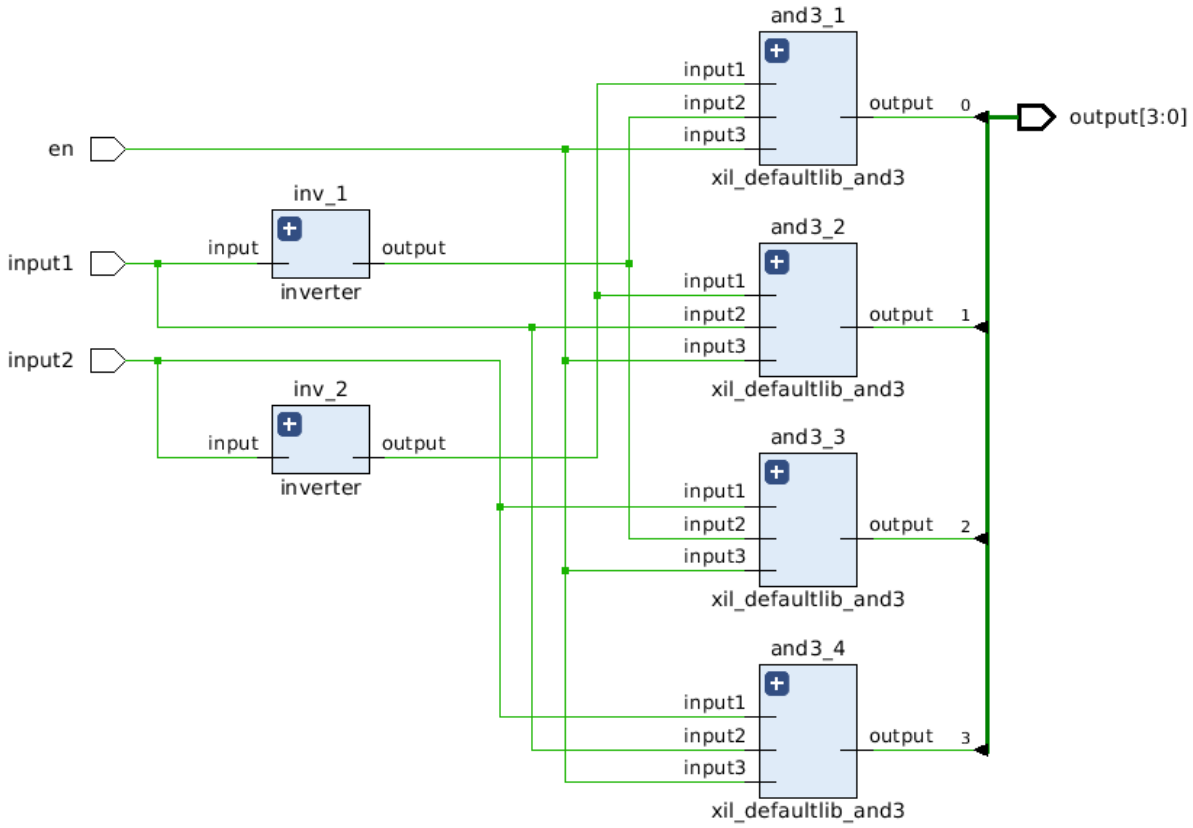
This block consists of the comparator logic using the XOR gate to compare the valid_tag address to the cpu address in order to determine the hit and miss operation.



Layout of Hit_miss block

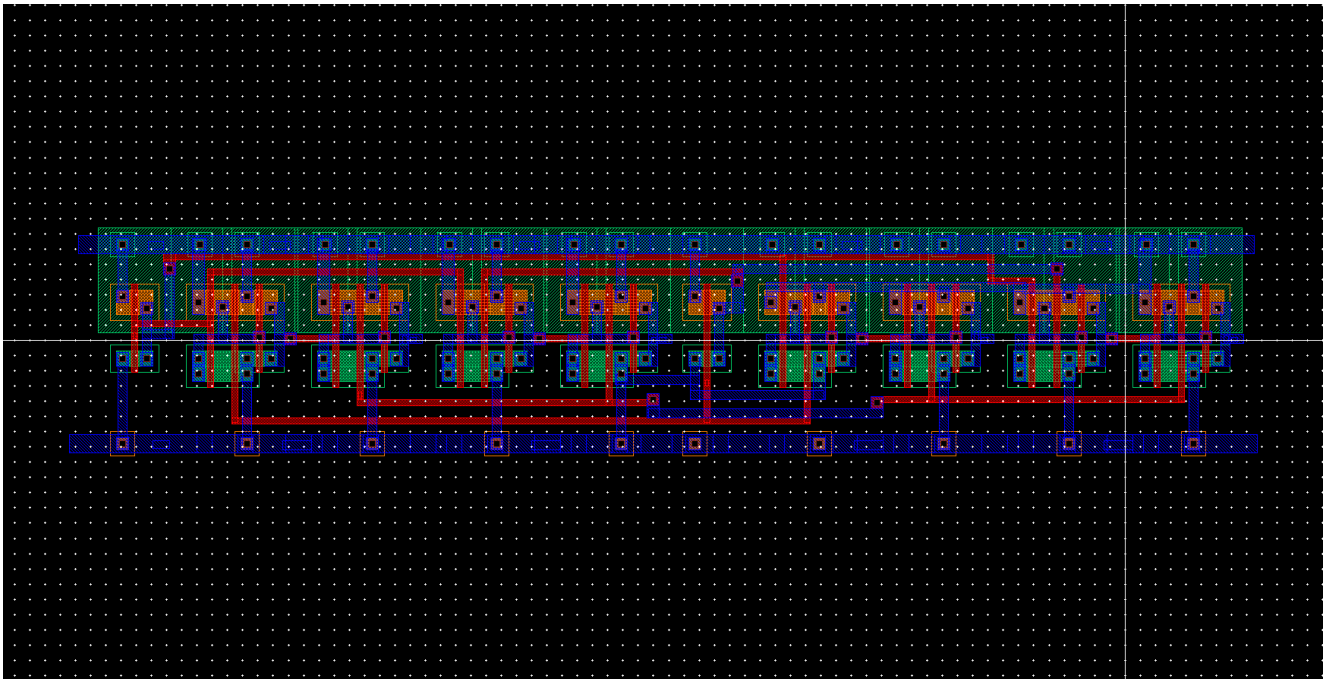


Decoder_2to4 Block :

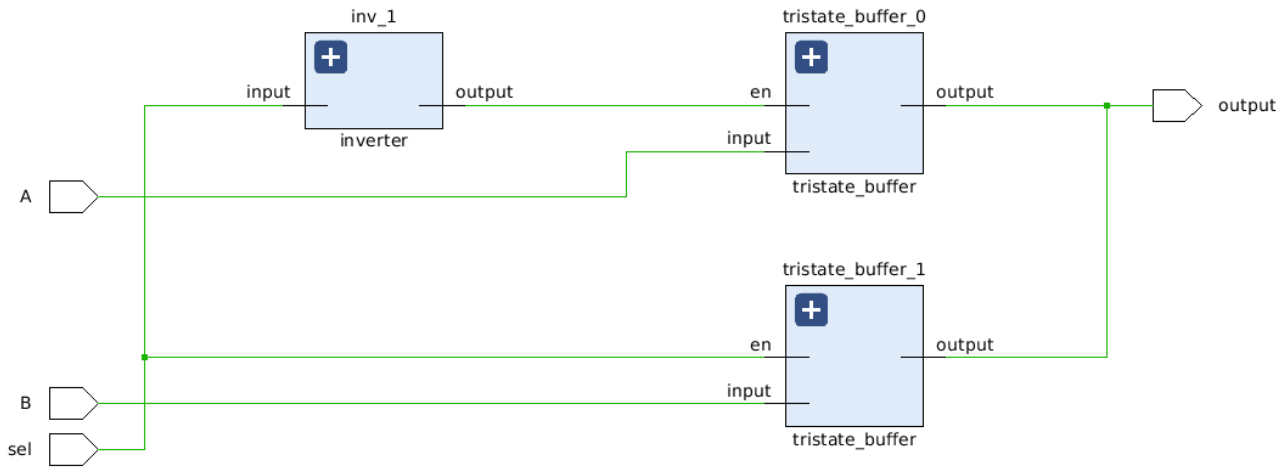


This block is used to decode the byte address from the cpu address.

Layout of Decoder_2to4 Block

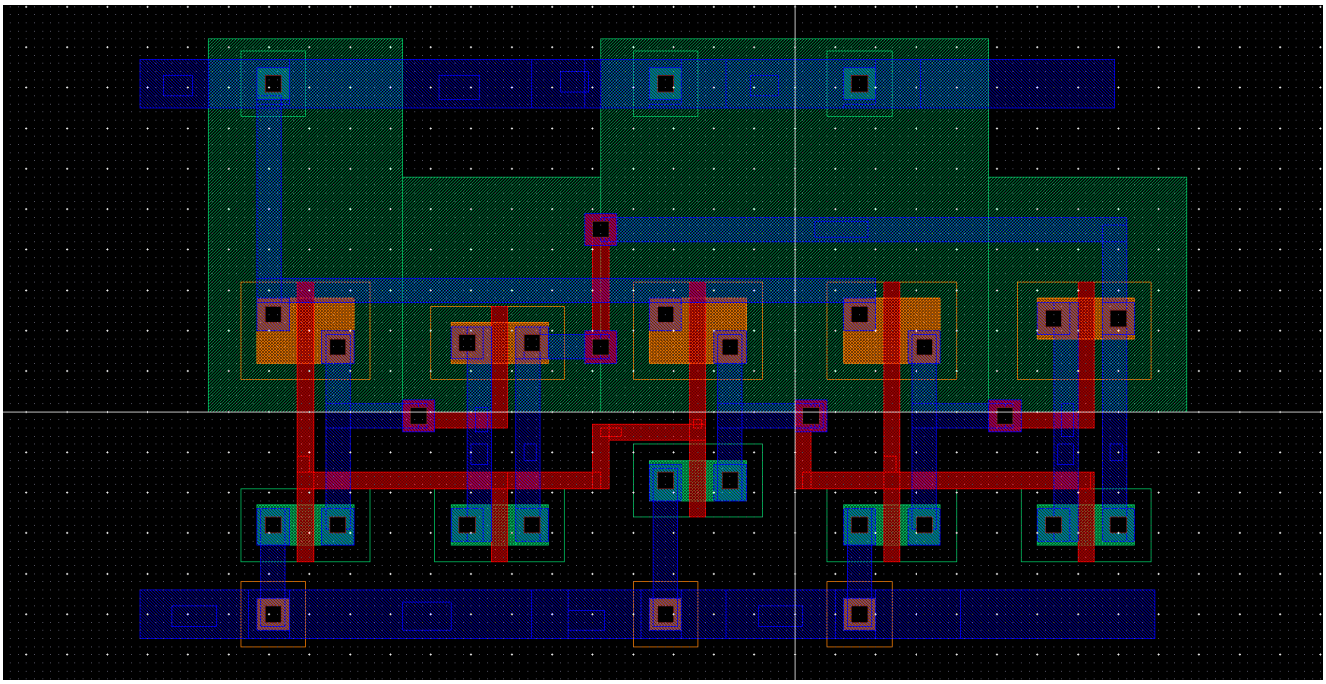


Mux_2to1 Block :



This block selects which signal will go to the cache block such as memory data or the cpu data based on the signal.

Layout of Mux_2to1 Block



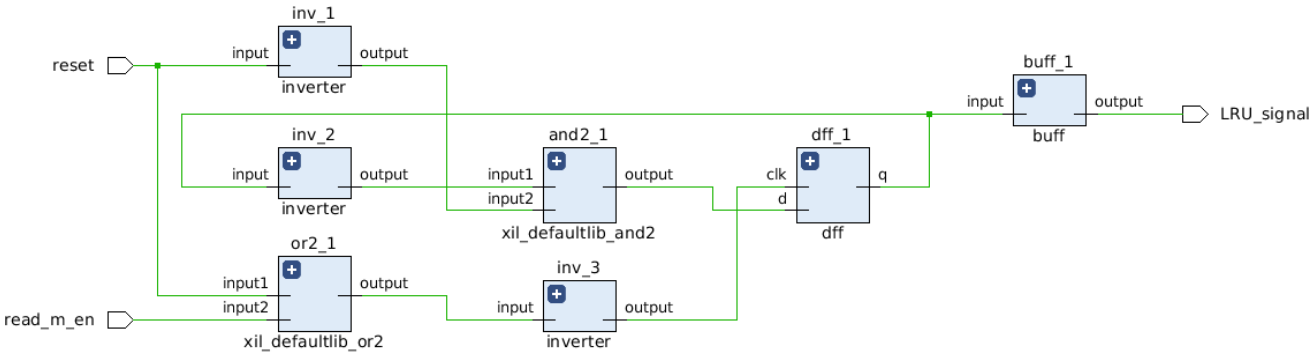
Part 3: Design of Least recent use (LRU)

In my 64 byte design, I have used the least recently used block (LRU) in order to determine the cache in case of miss_read operation.

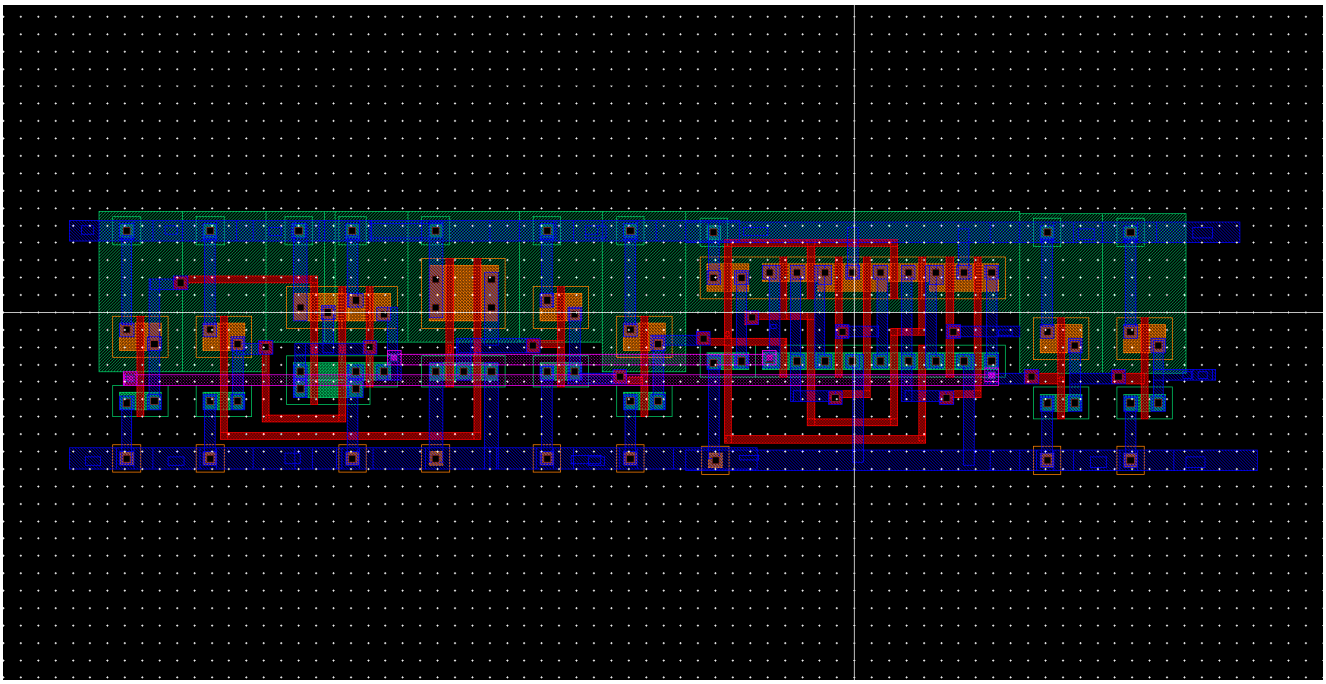
This is build

- DFF to hold the state
- And some primitive cell for logical computation

The reset signal will make the LRU to 0, which will select the Cache_block0, and when a read_miss operation is executed it will change to the opposite state. For example, if it is 0, it will change to 1 and vice versa.
1 value corresponds to Cache_block1.

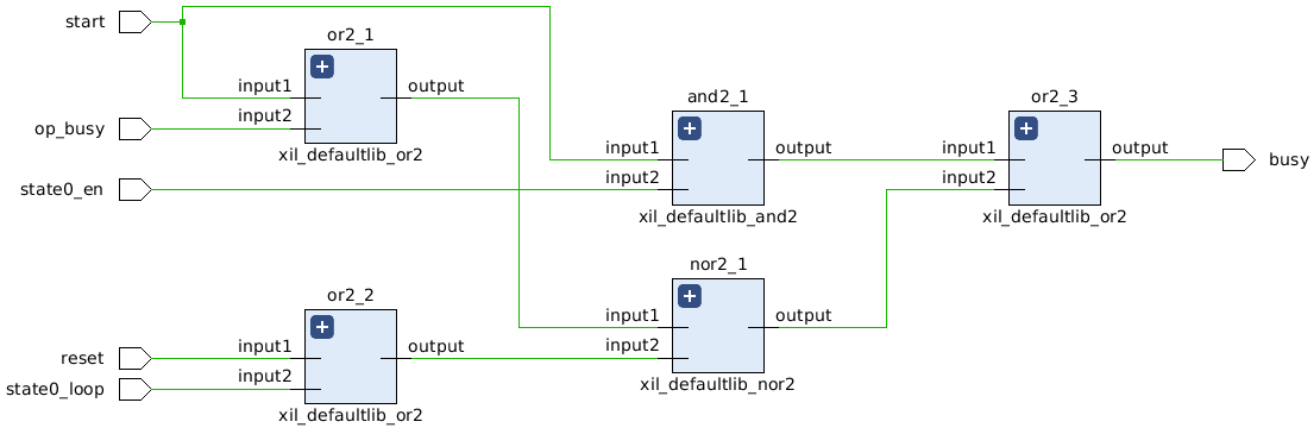


Layout of LRU Block

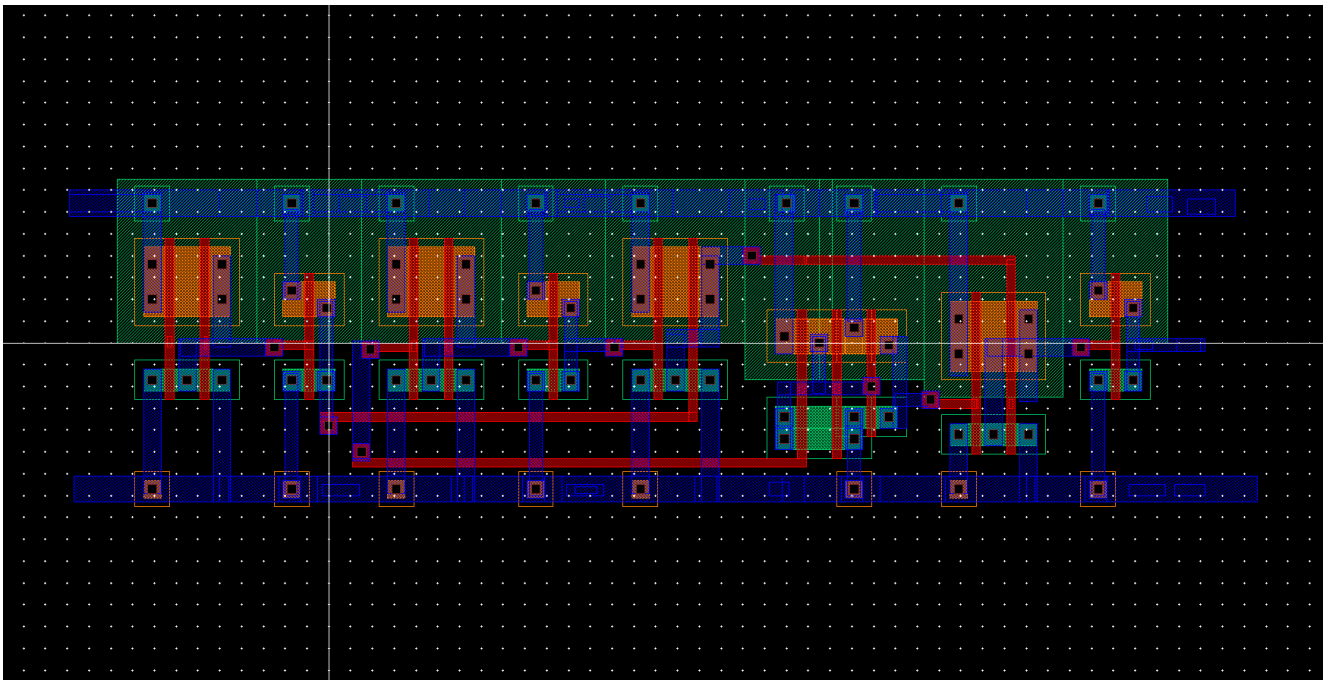


Part 4: Design of busy_block

The busy block is used to set the handshaking signal high during any operation. The busy block sets high when the start signal is placed and remains high until an operation is done.
The busy block consists of mainly the primitive cell as shown in the following figure.

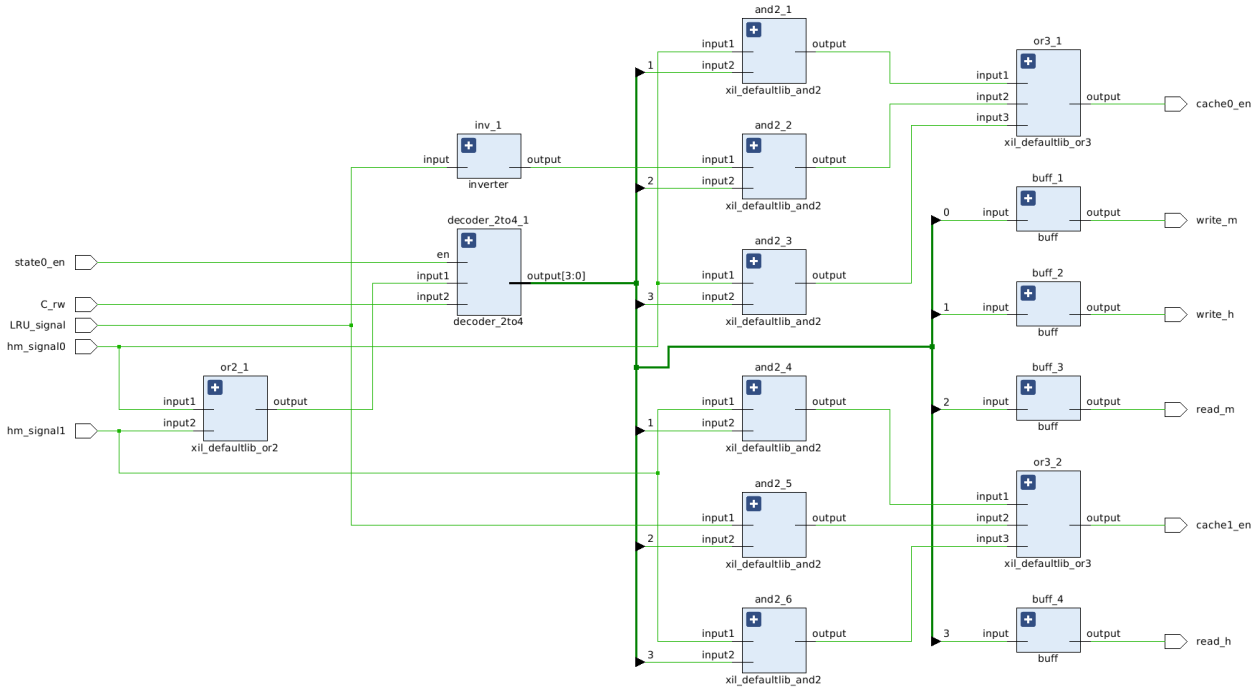


Layout of busy Block

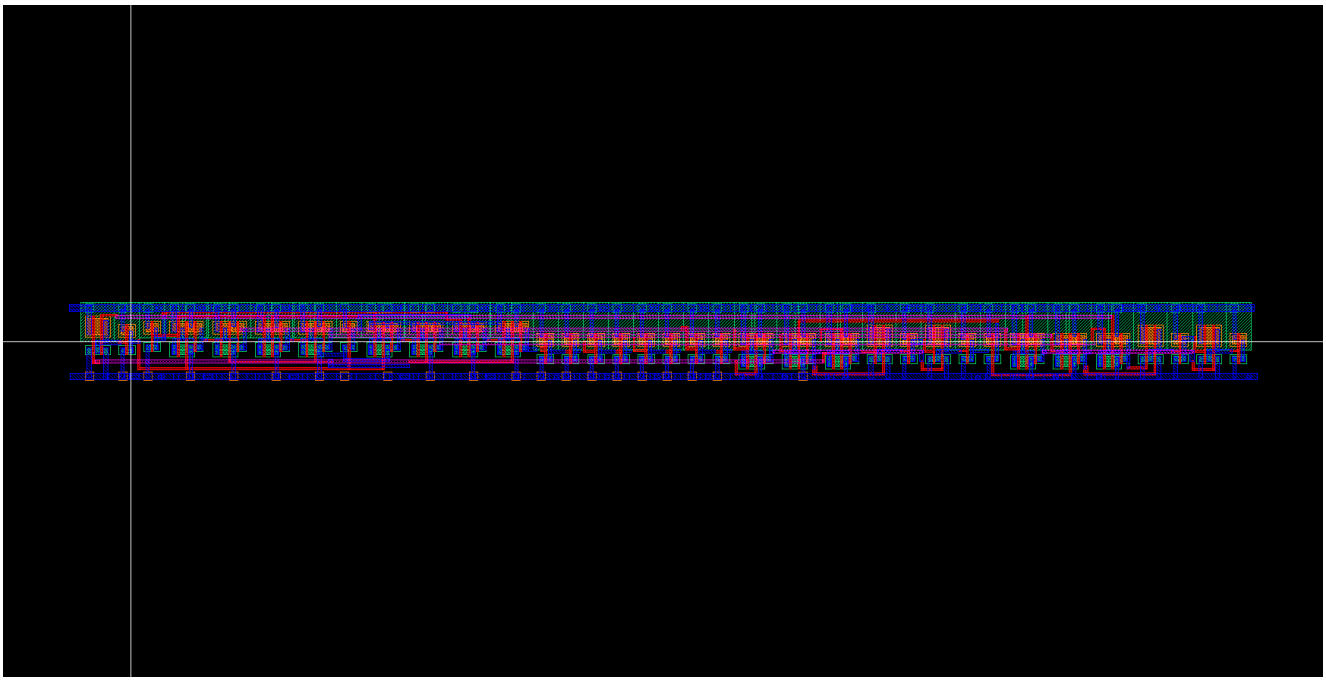


Part 5: Design of control block

The control block determines from which cache block the hit signal is coming and turns on that cache block and suppresses the other. It is also determined which block has the read miss based on the LRU signal. The control block consists of a decoder block and some primitive gates as shown in the following figure.

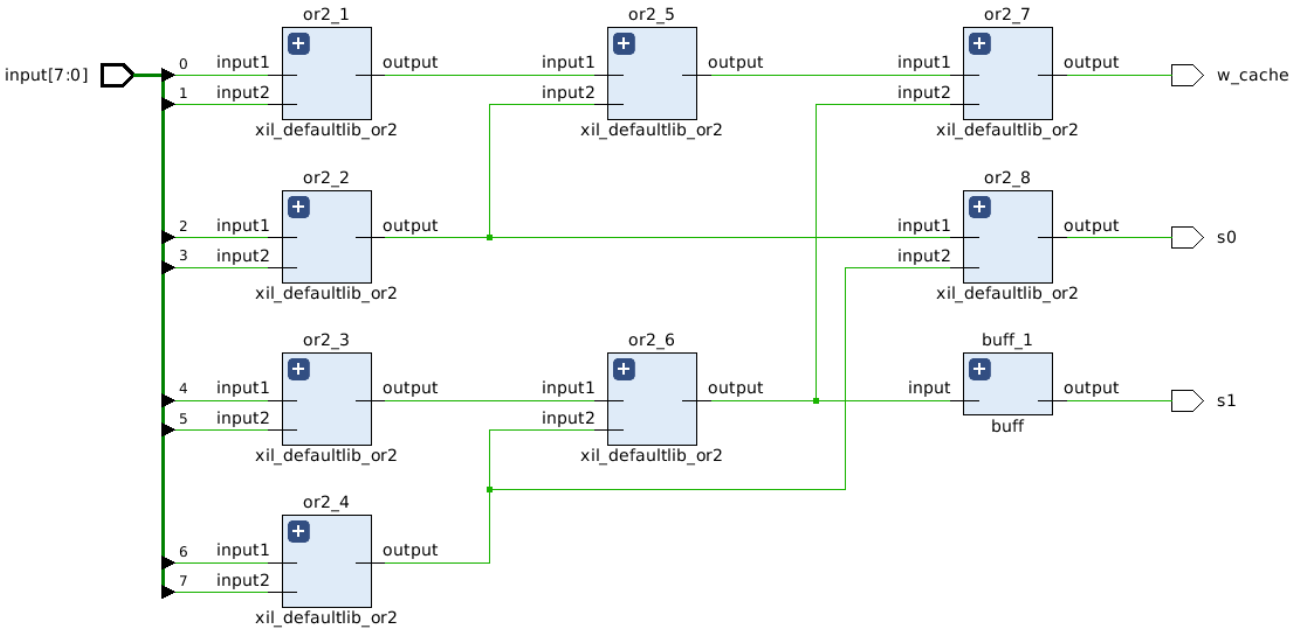


Layout of control block

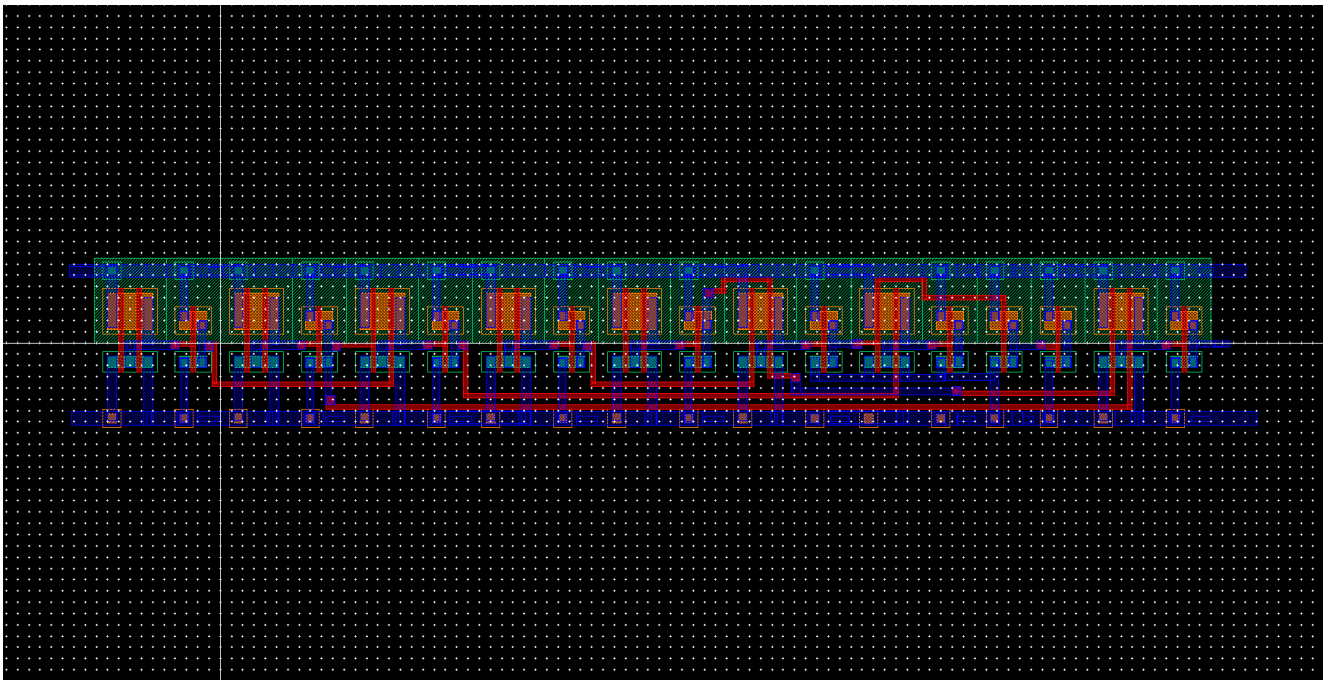


Part 6: Design of read_miss_control block

When the read miss occurs, then this read_miss control block receives the signal from the state machine from the 8 clock cycle to 14 block cycle to determine which byte the cache memory needs to write. With the help of the primitive logic cell and the encoder block, it refers to the byte 00 to 11.


input[7:0]
0
1
2
3
4
5
6
7
or2_1
or2_2
or2_3
or2_4
or2_5
or2_6
or2_7
or2_8
buff_1
input1
input2
output
input
xil_defaultlib_or2
buff
w_cache
s0
s1

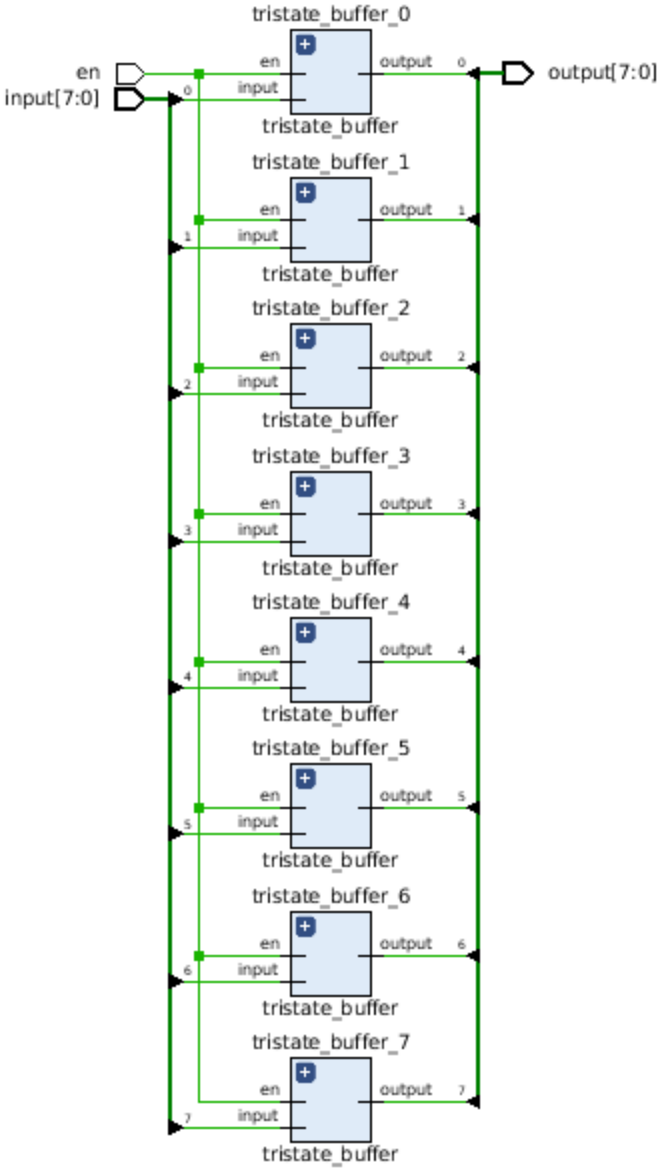
Layout of control block

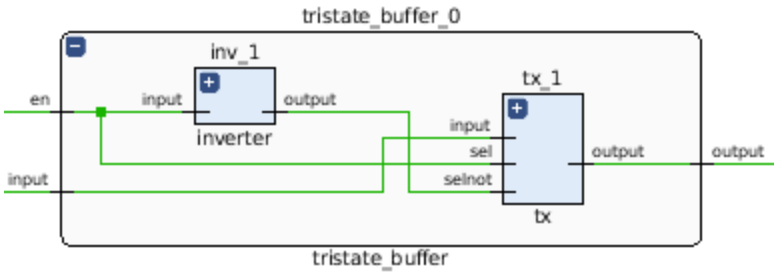


Part 7: Design of tri_state_buffer, register, and decoder block

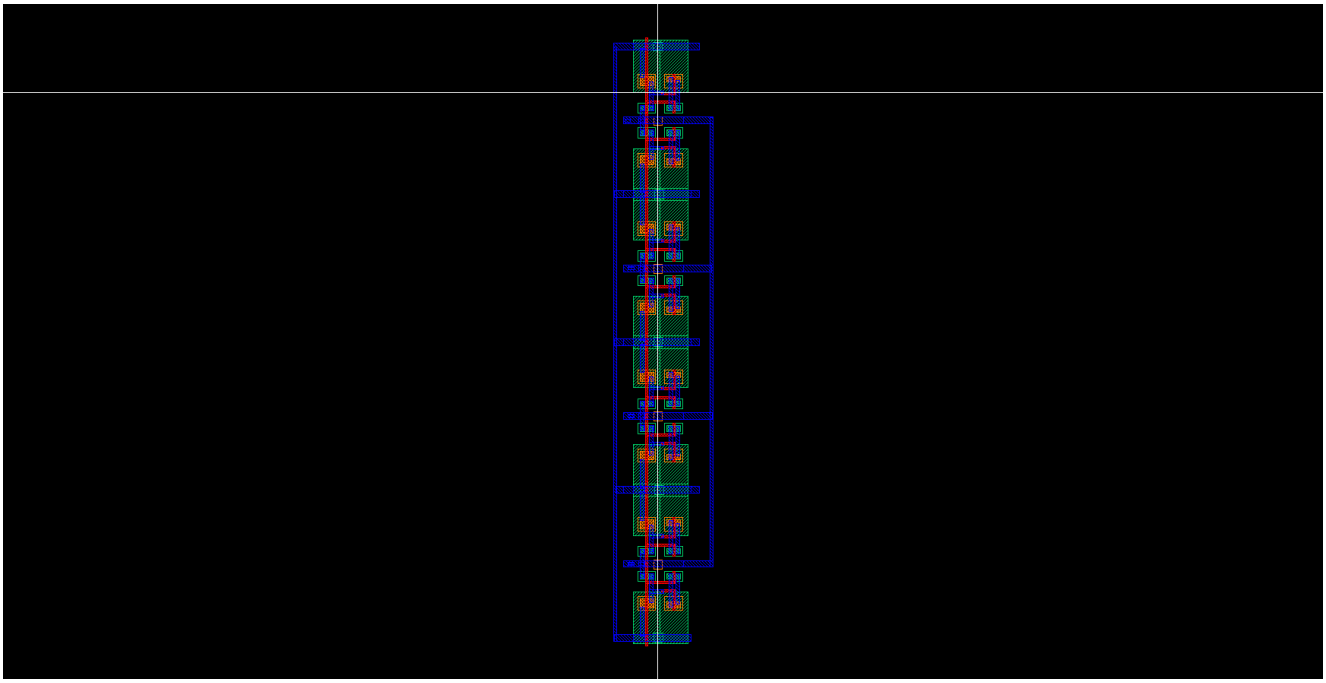
Tri_state_buffer

The tri_state_buffer is used to deliver the output in the control way when it is enabled to pass the output and Z on the other time.

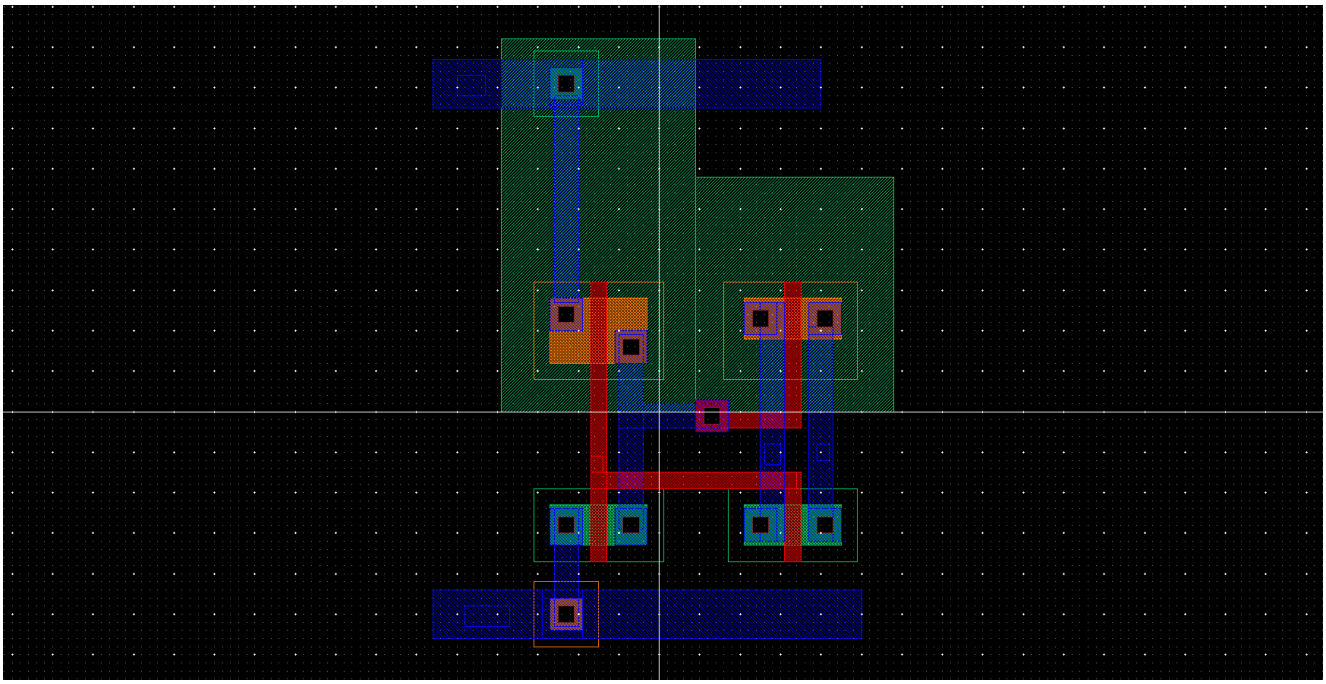




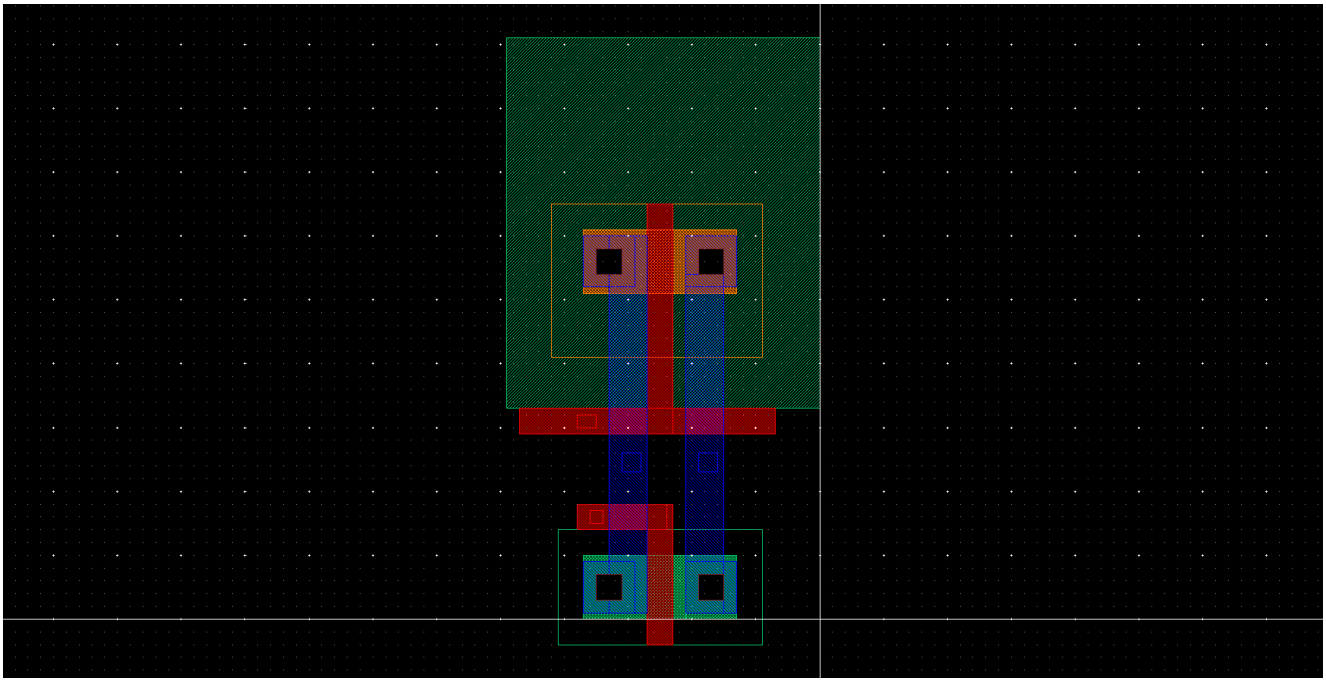
Layout of Tri_state_buffer (byte cell)



Layout of Tri_state_buffer (bit cell)

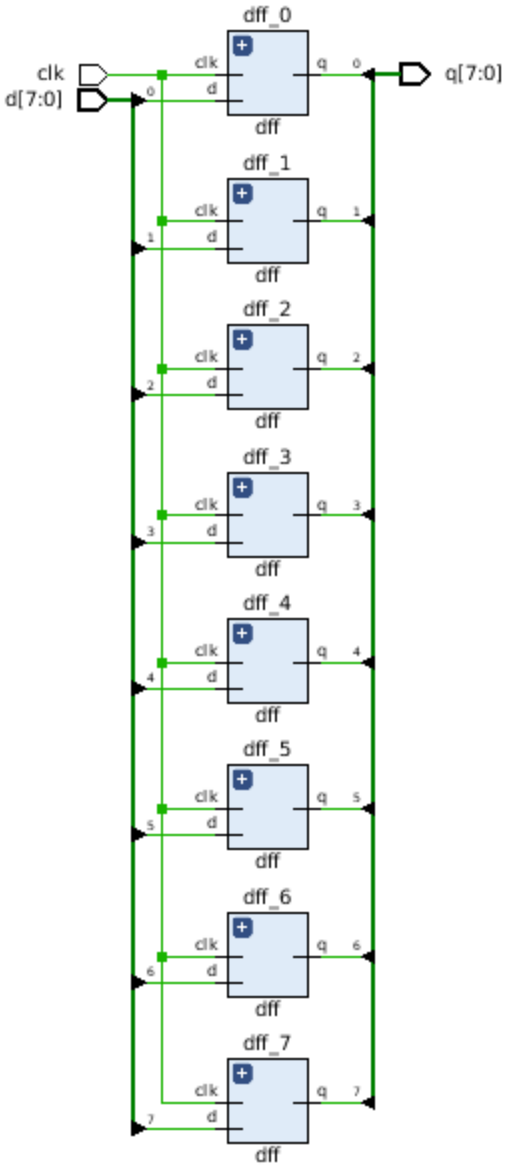


Layout of Tri_state_buffer (transmission gate)

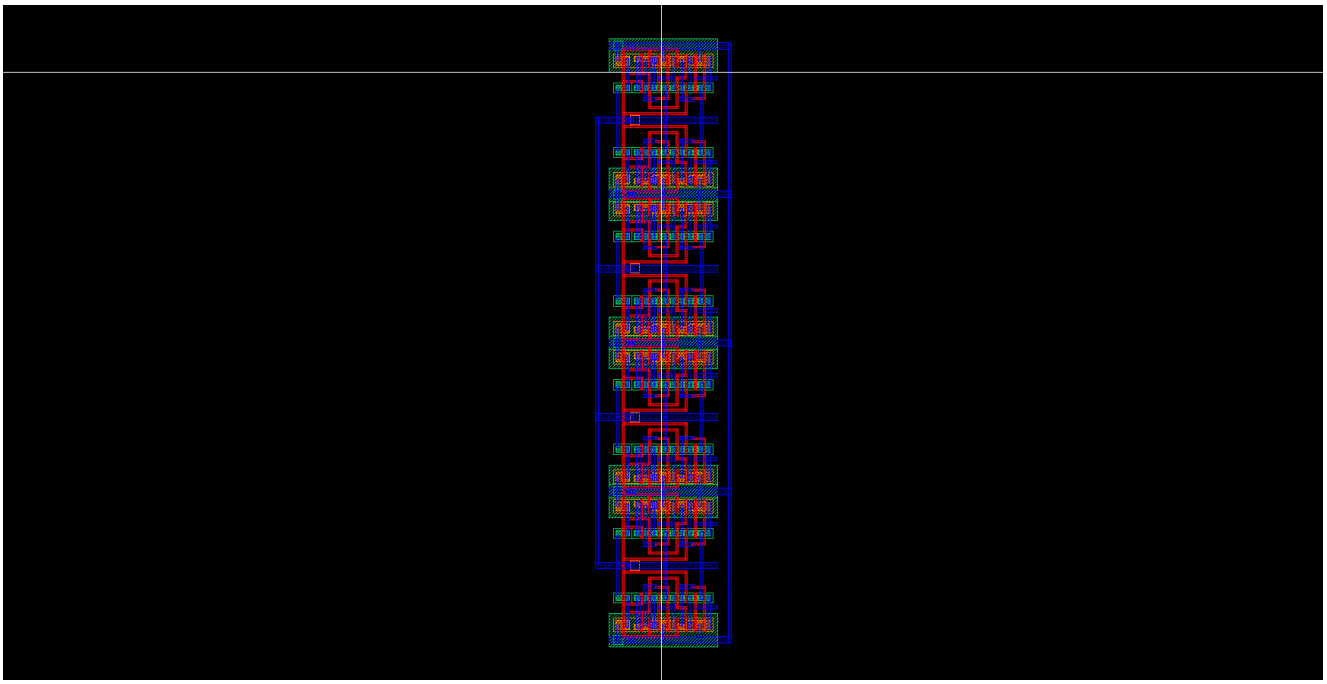


Register

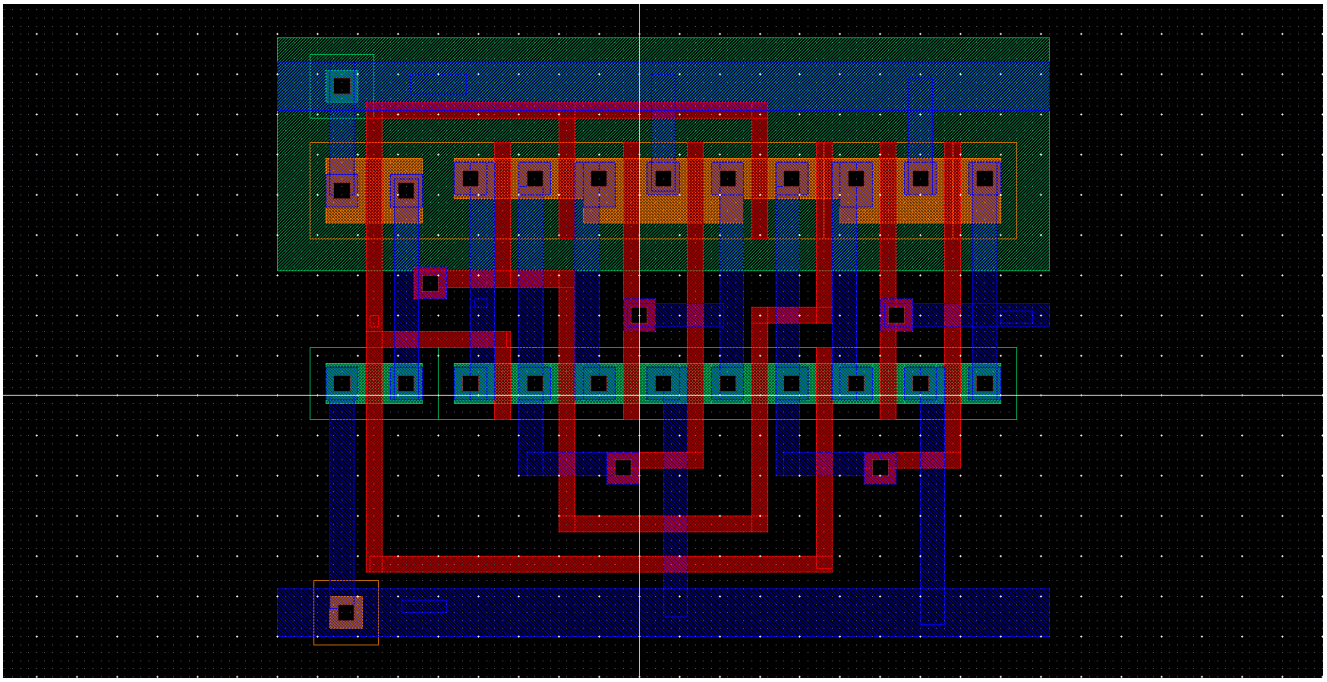
This is used to register the input and in out signal. Particularly, the cpu address, cpu data, and the cpu read-write signal. The blocks are shown as follows.



Layout of Register(byte cell)

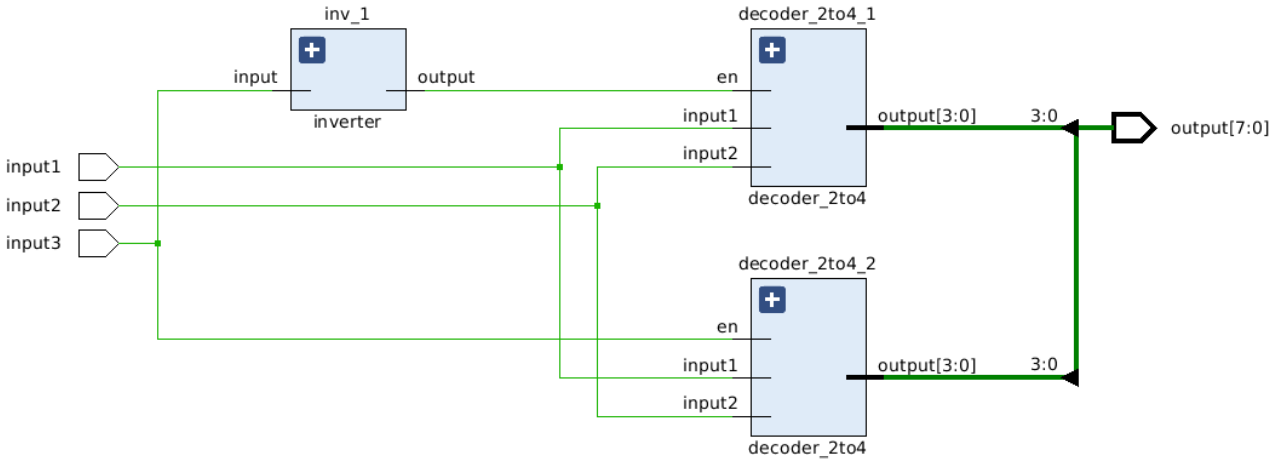


Layout of Register(bit cell)

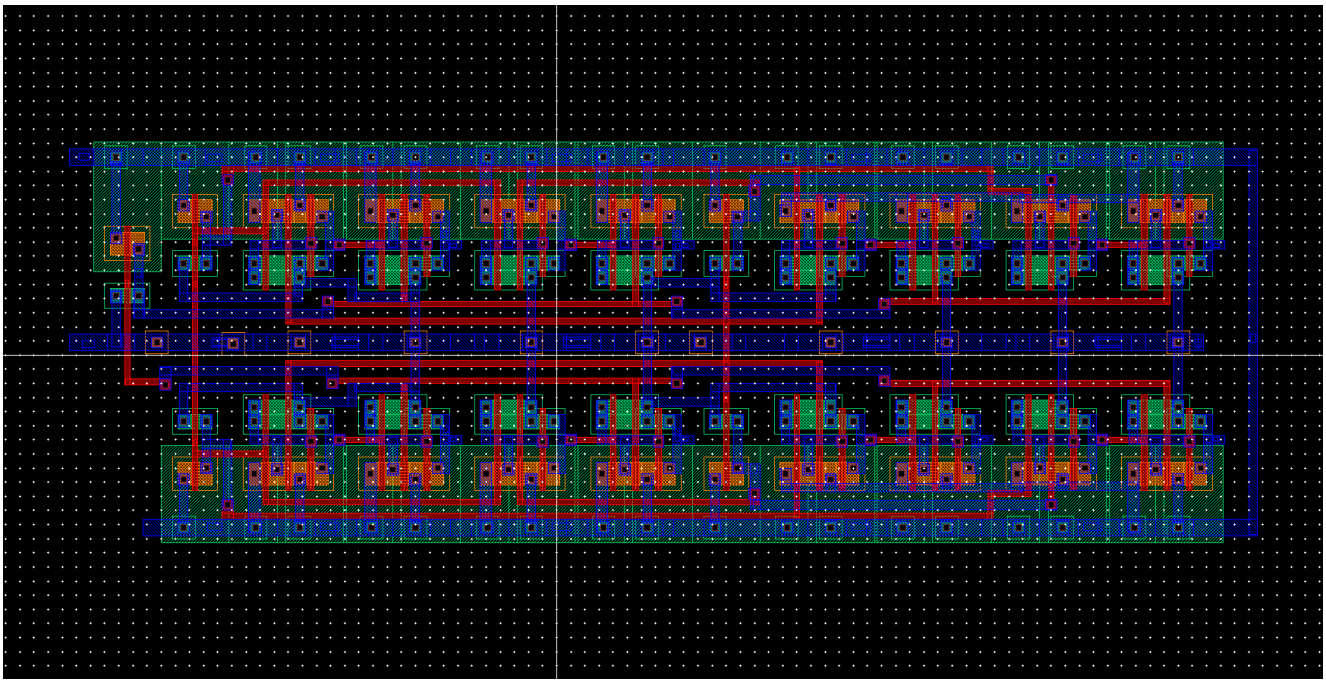


Decoder Block

The 3 to 8 bit decoder is used to decode the block address, which consists of the two 2 to 4 decoders as shown below.

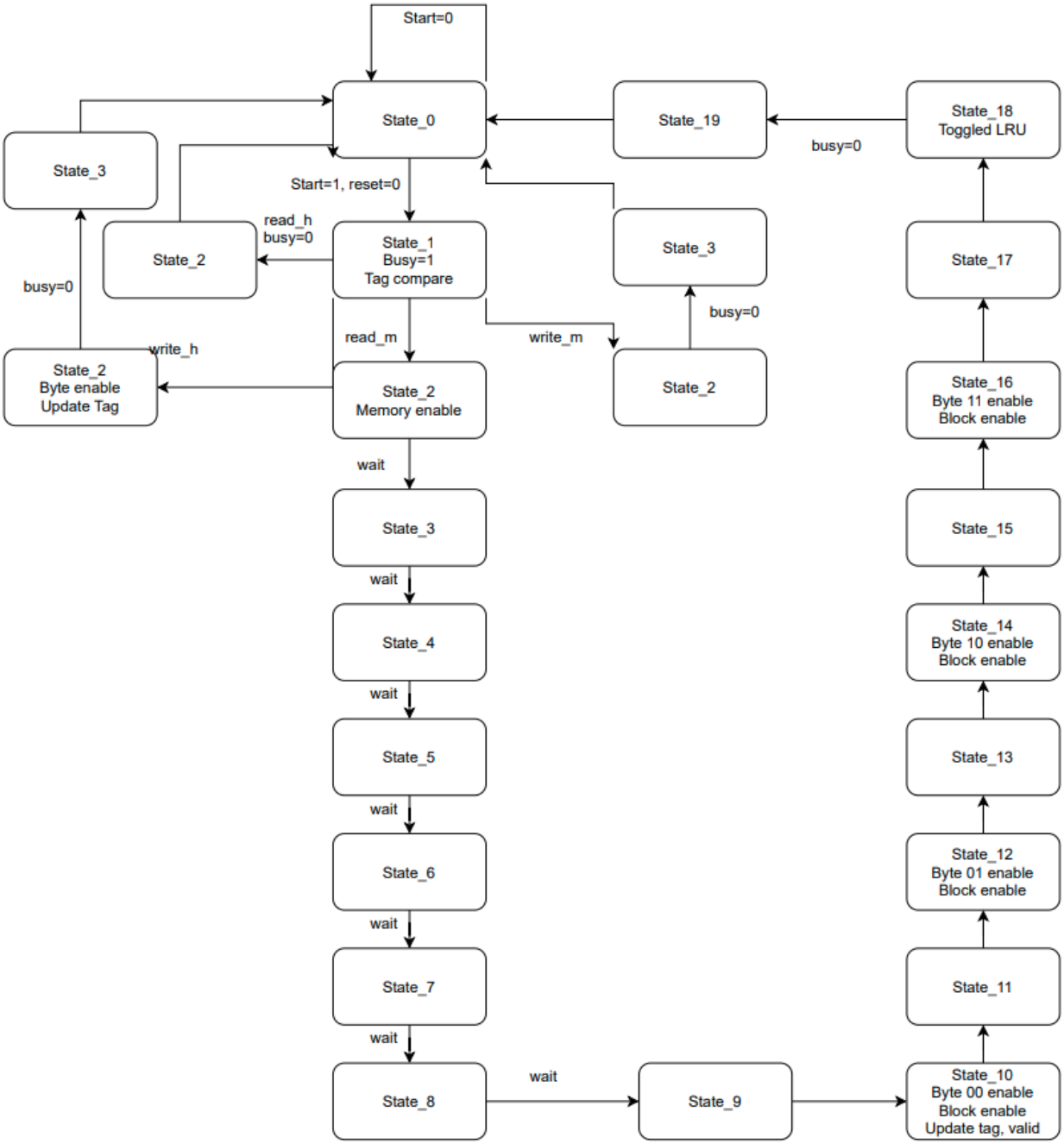


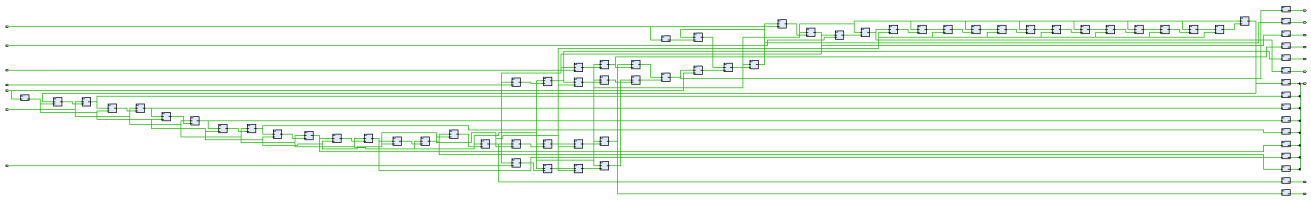
Layout of Decoder Block



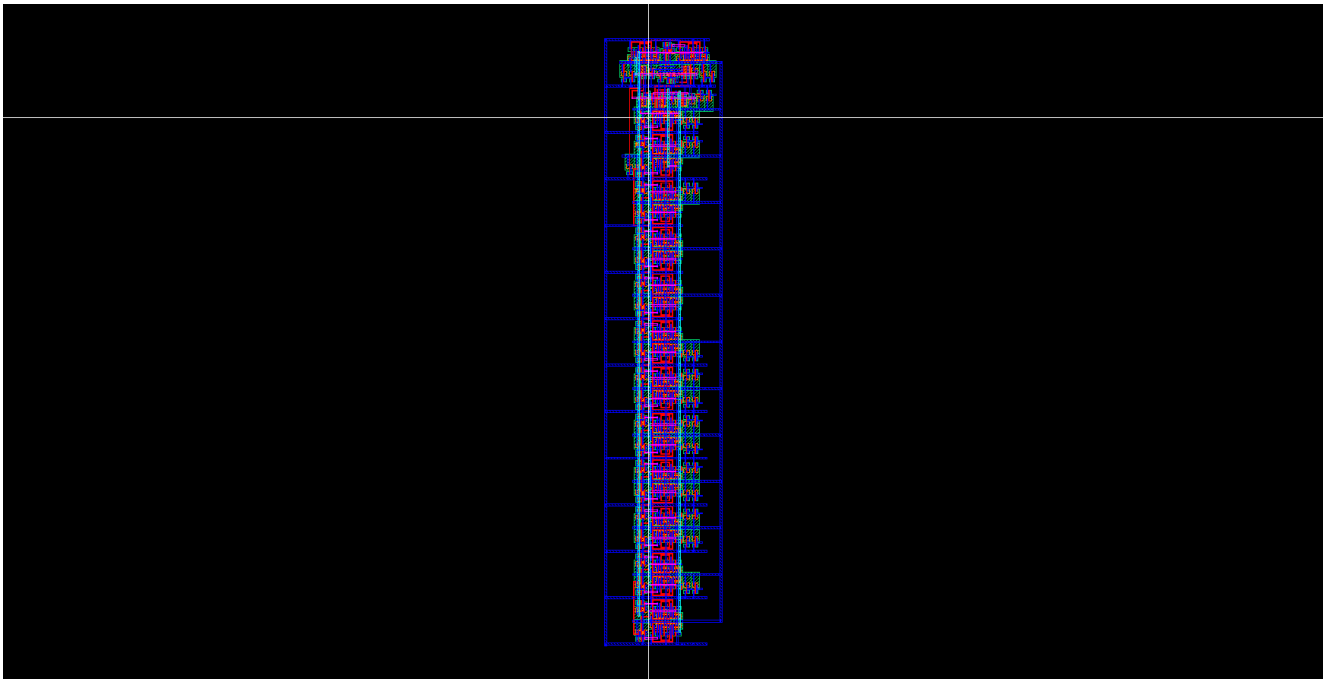
Part 8: Design of State control

The heart of the operation in the Cache chip is the state machine which sends control signals to all other blocks and builds with the shift register for my case. The state machine is built with primitive gates and the DFF.



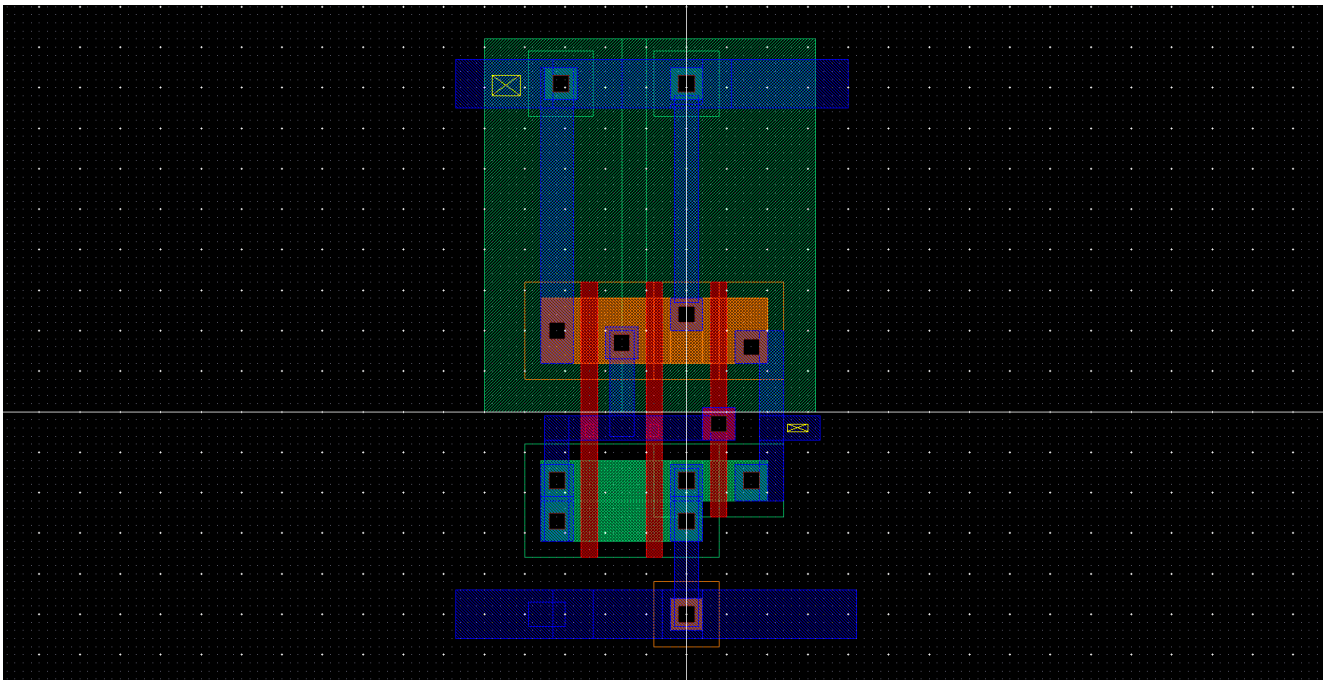


Layout of state machine

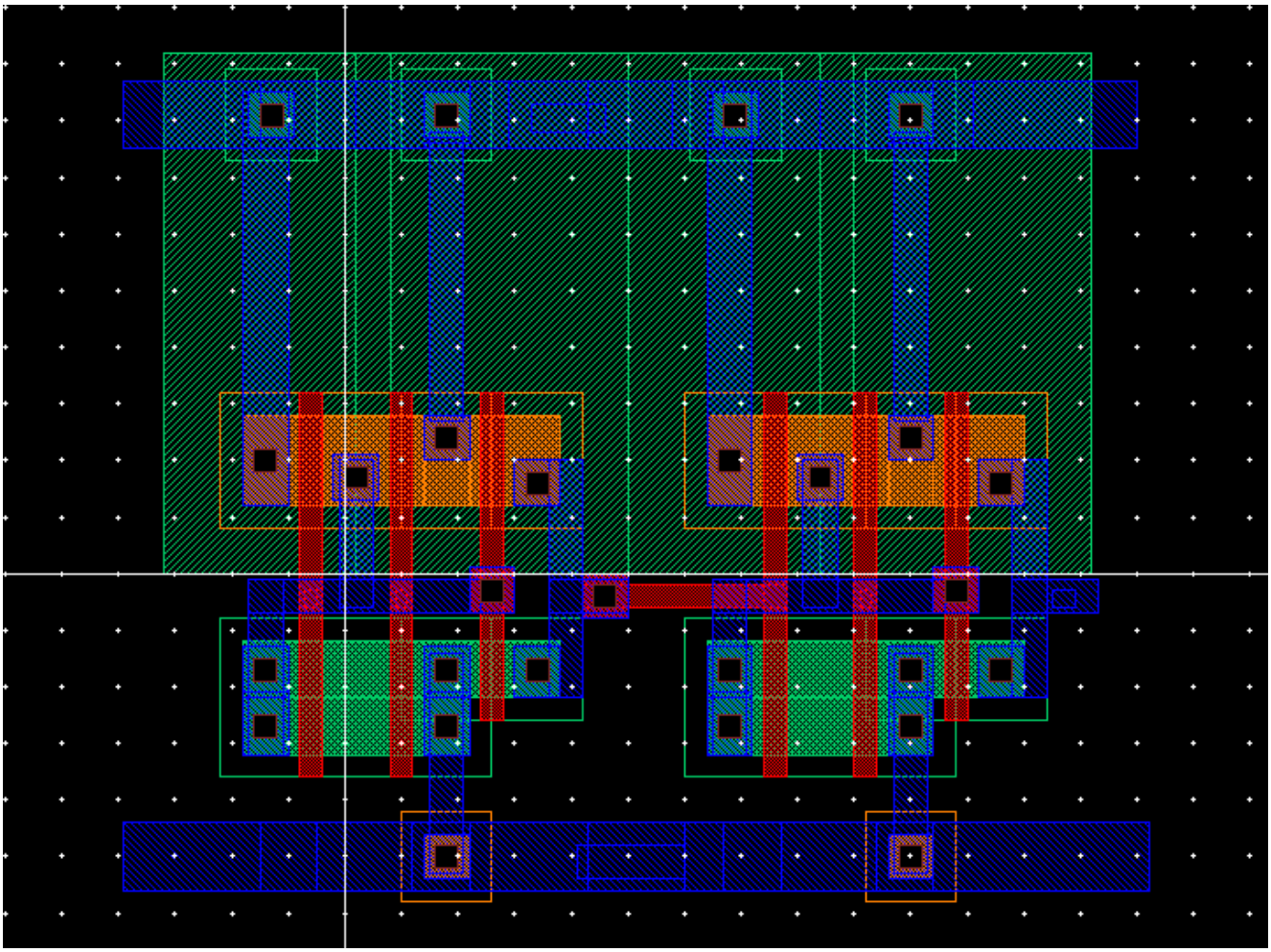


Part 9: Layout of miscellaneous cell

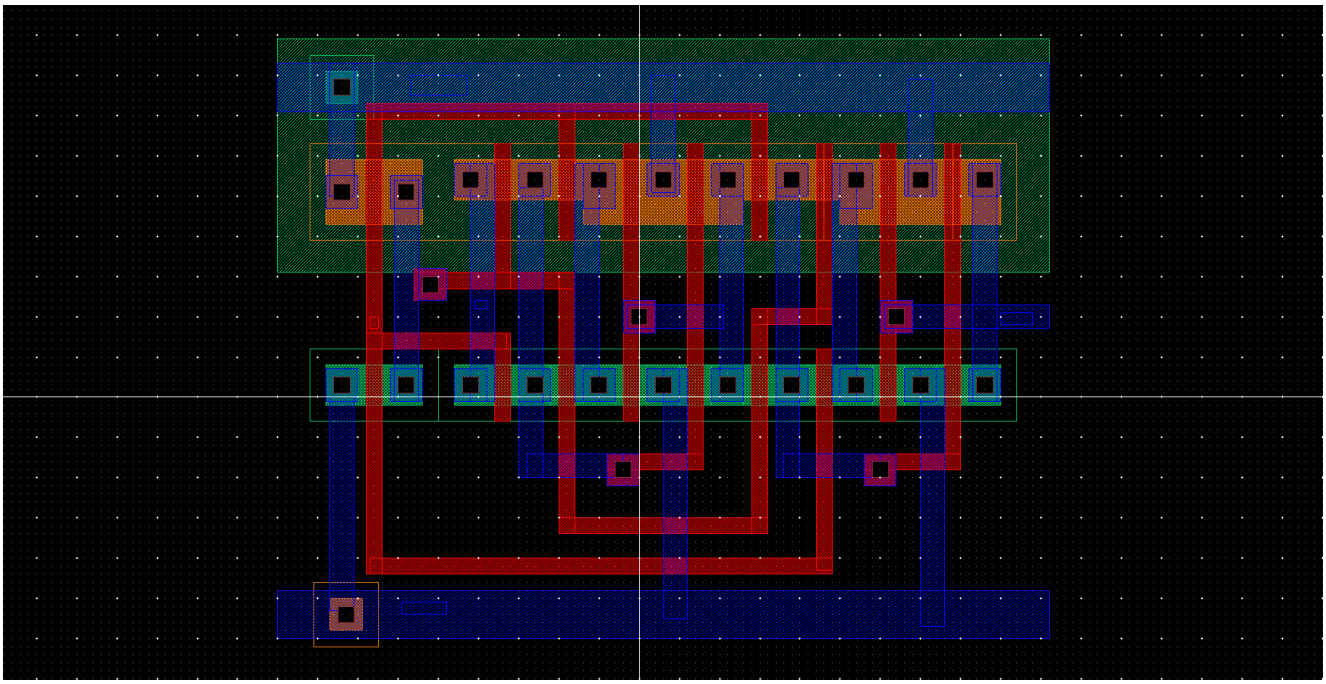
Layout of and2



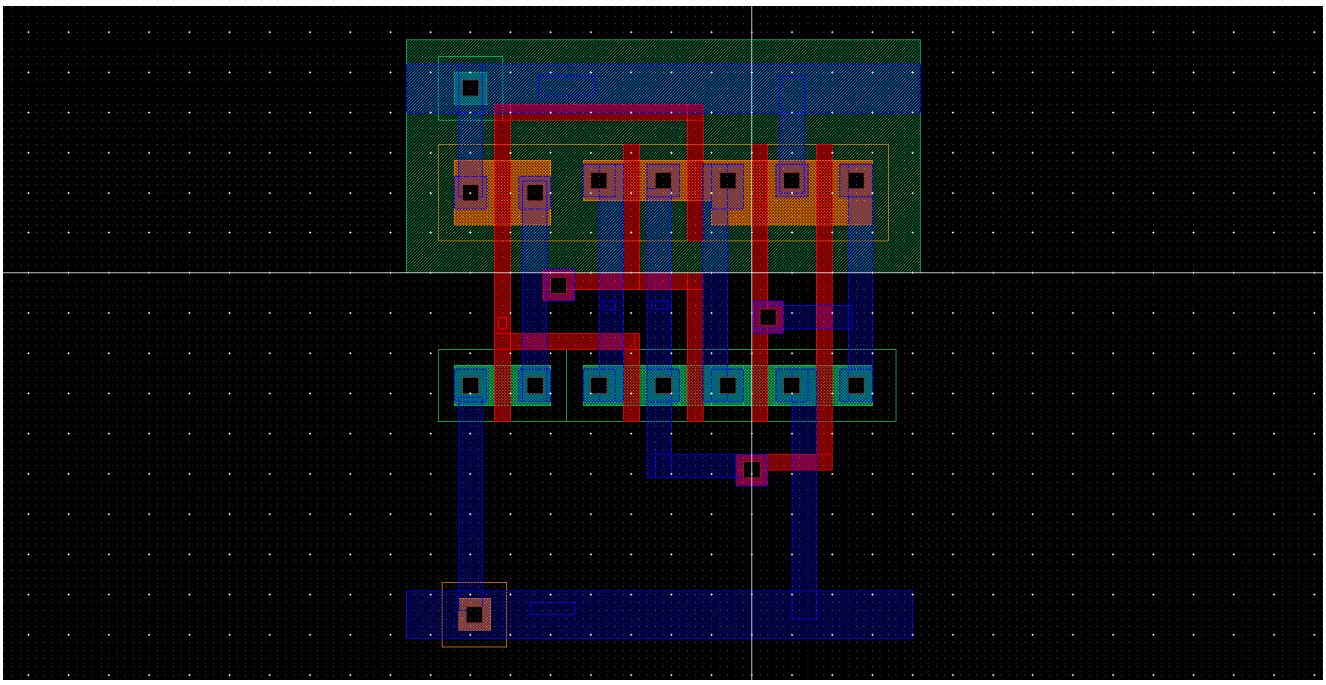
Layout of and3



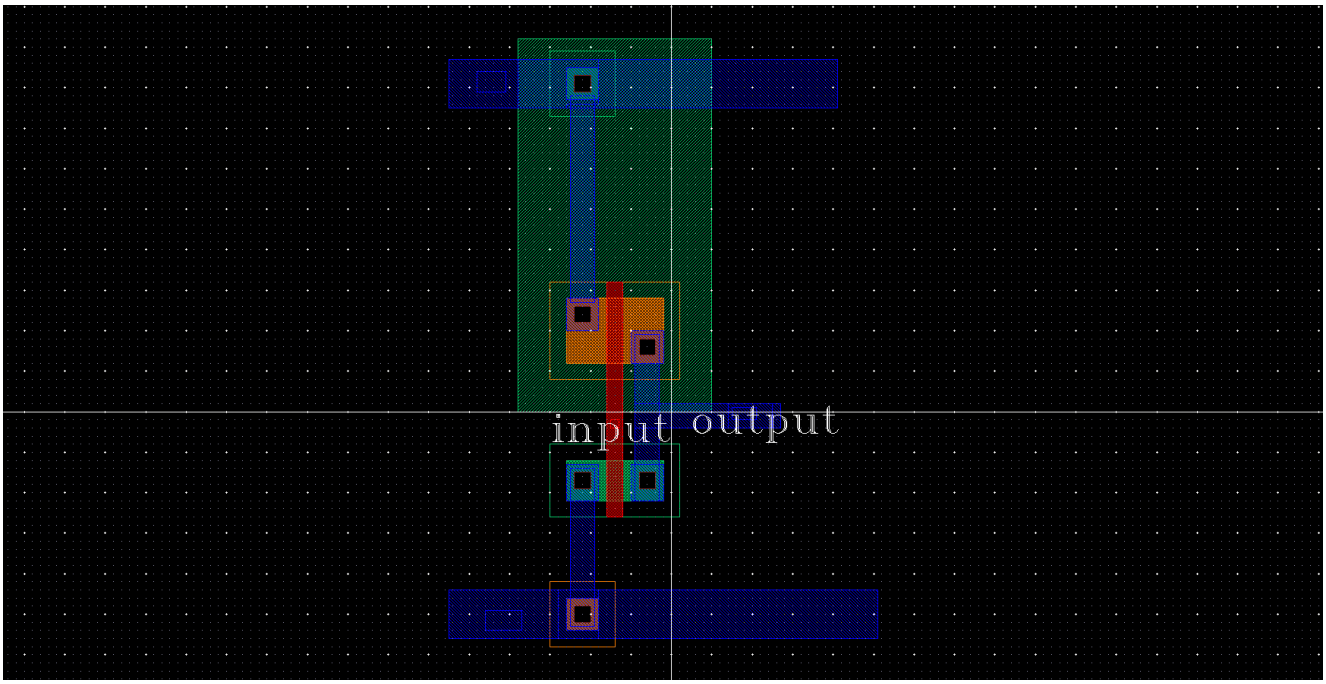
Layout of DFF



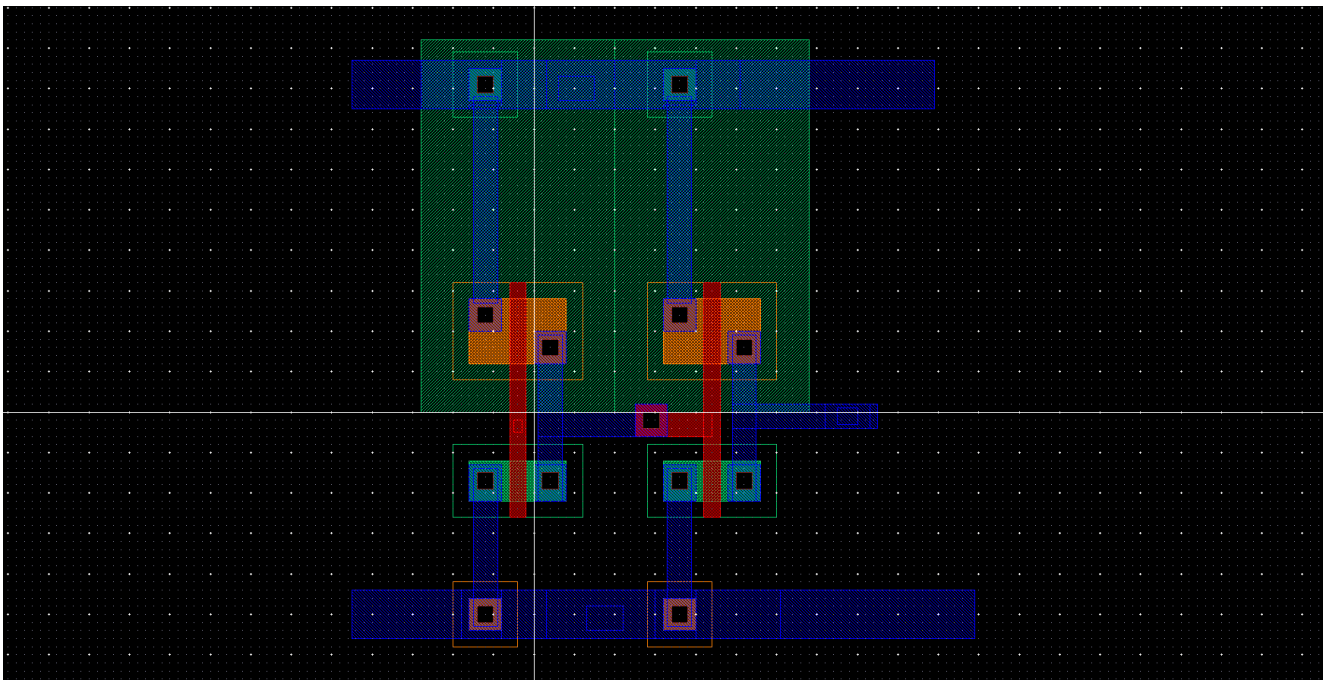
Layout of DLatch



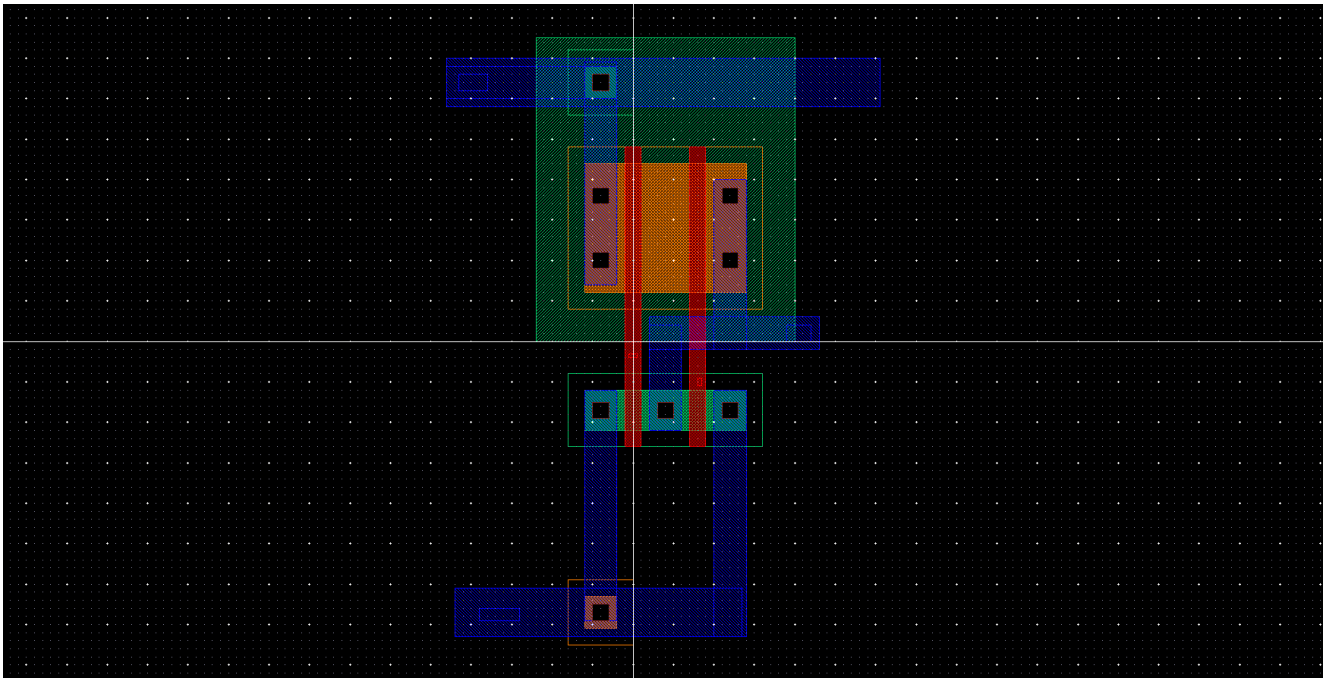
Layout of inverter



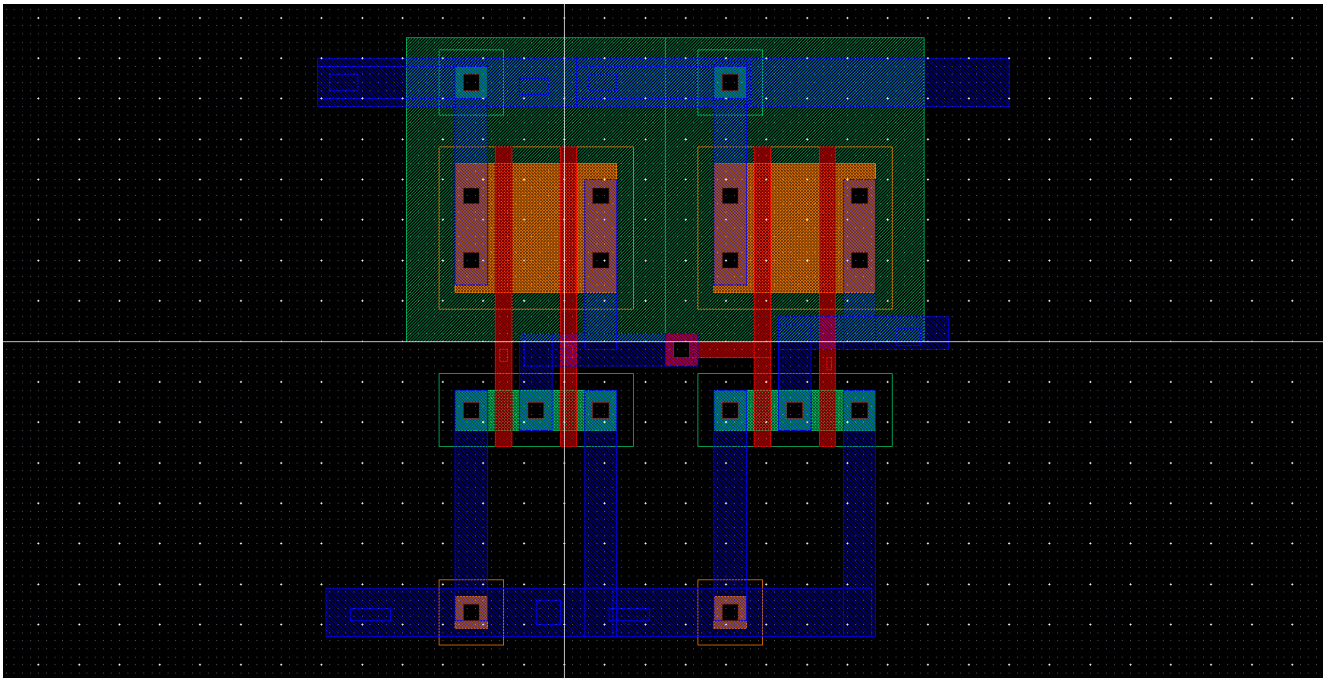
Layout of buffer



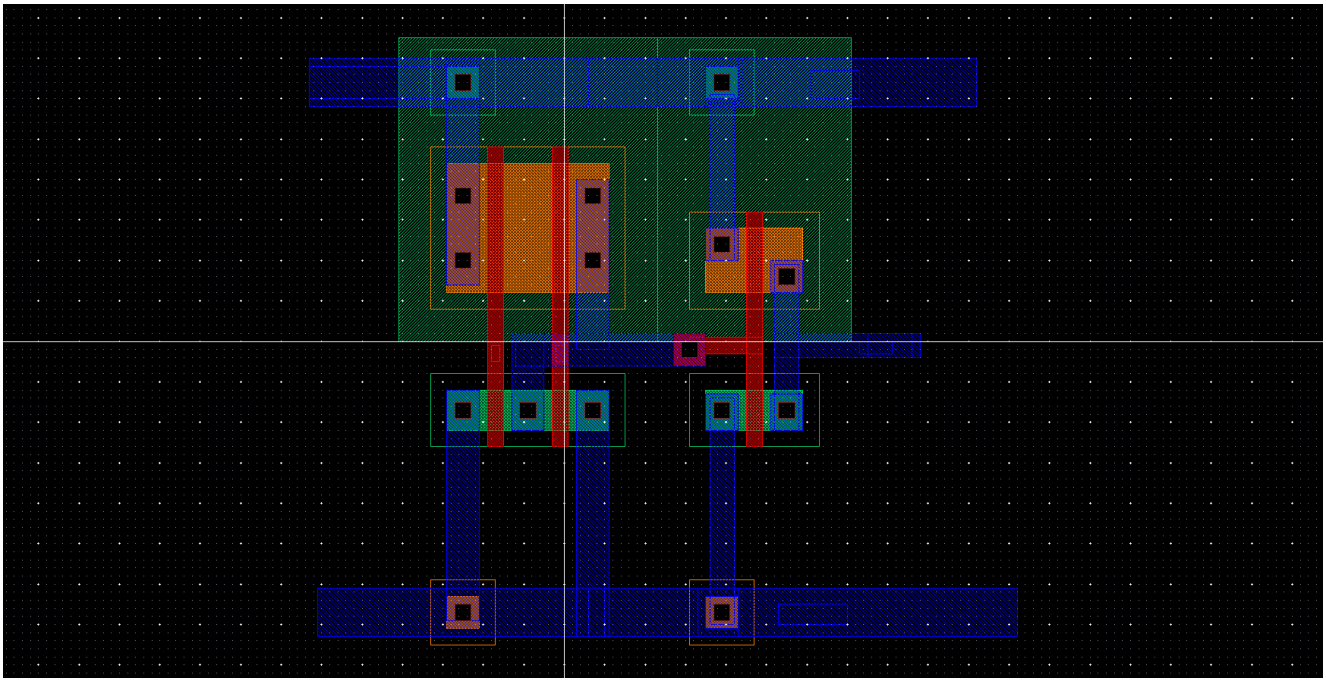
Layout of nor2



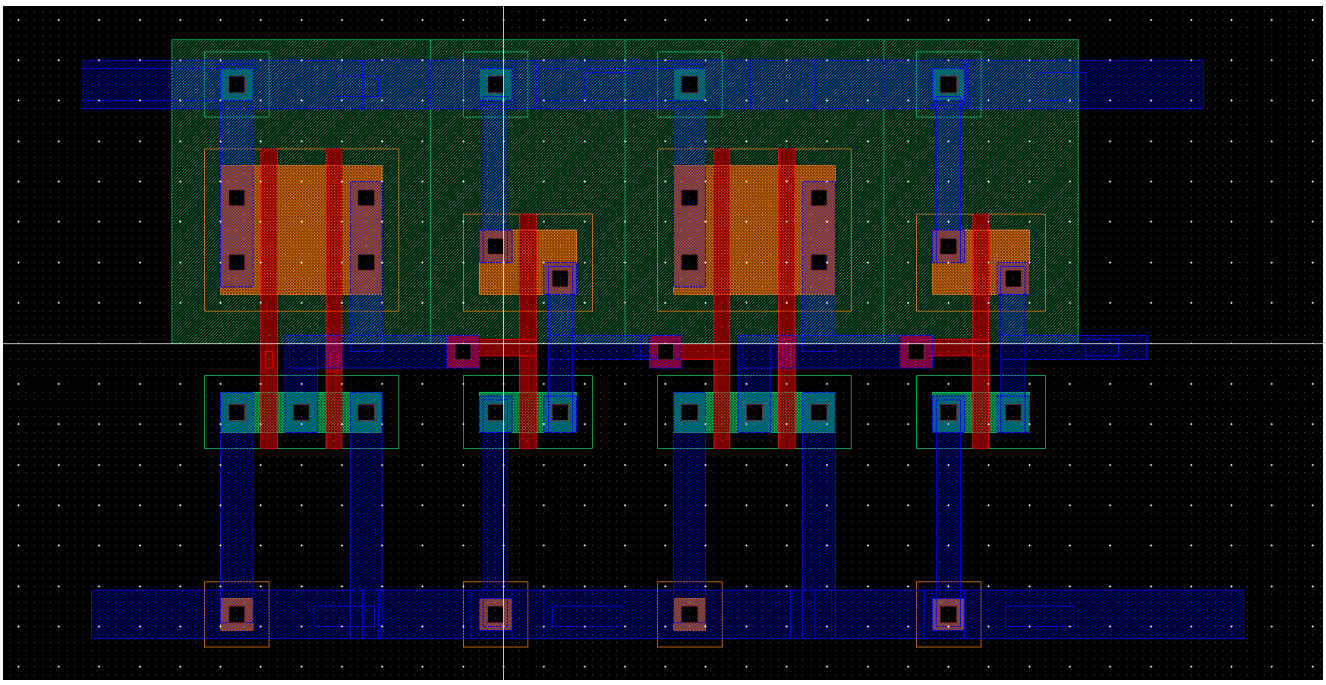
Layout of nor3



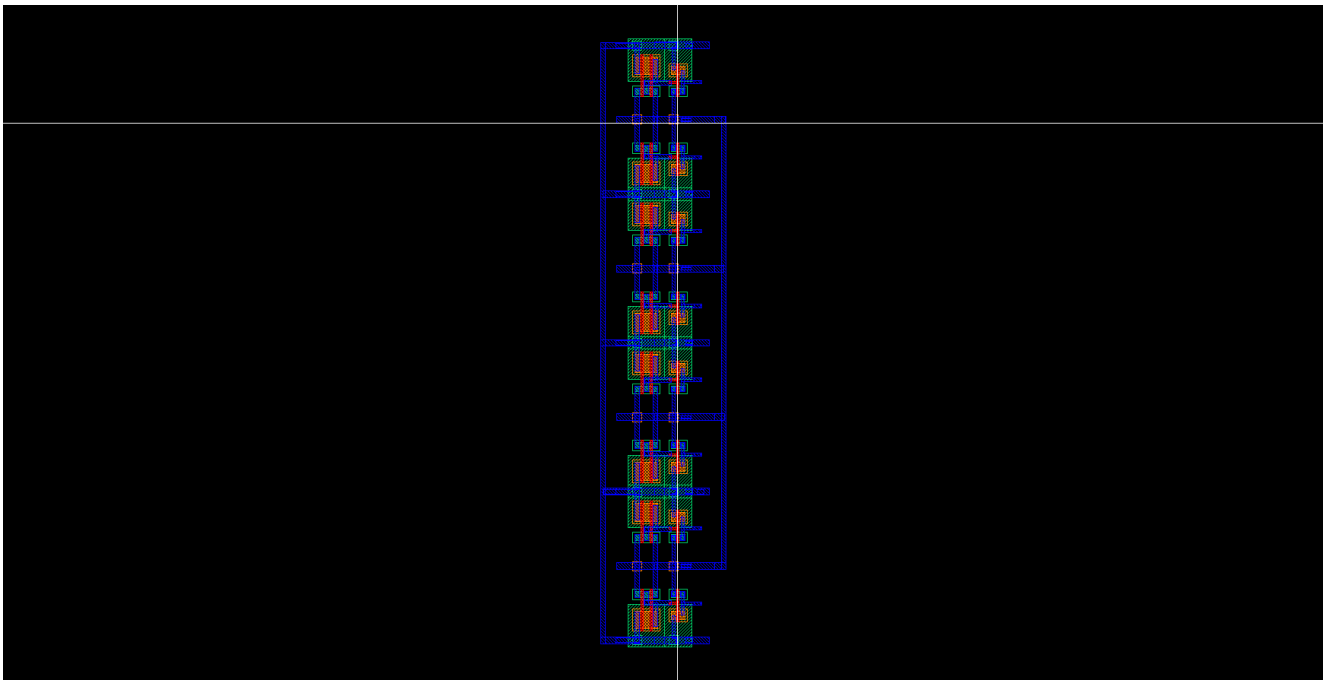
Layout of or2



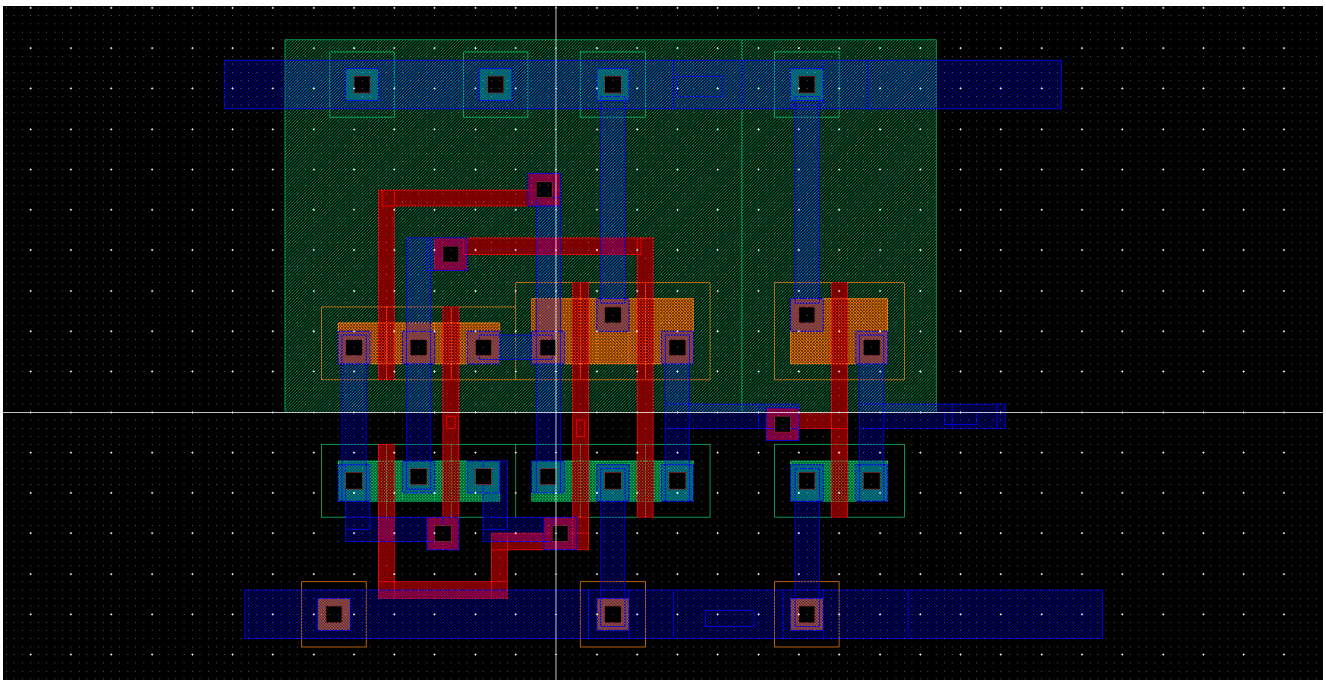
Layout of or3



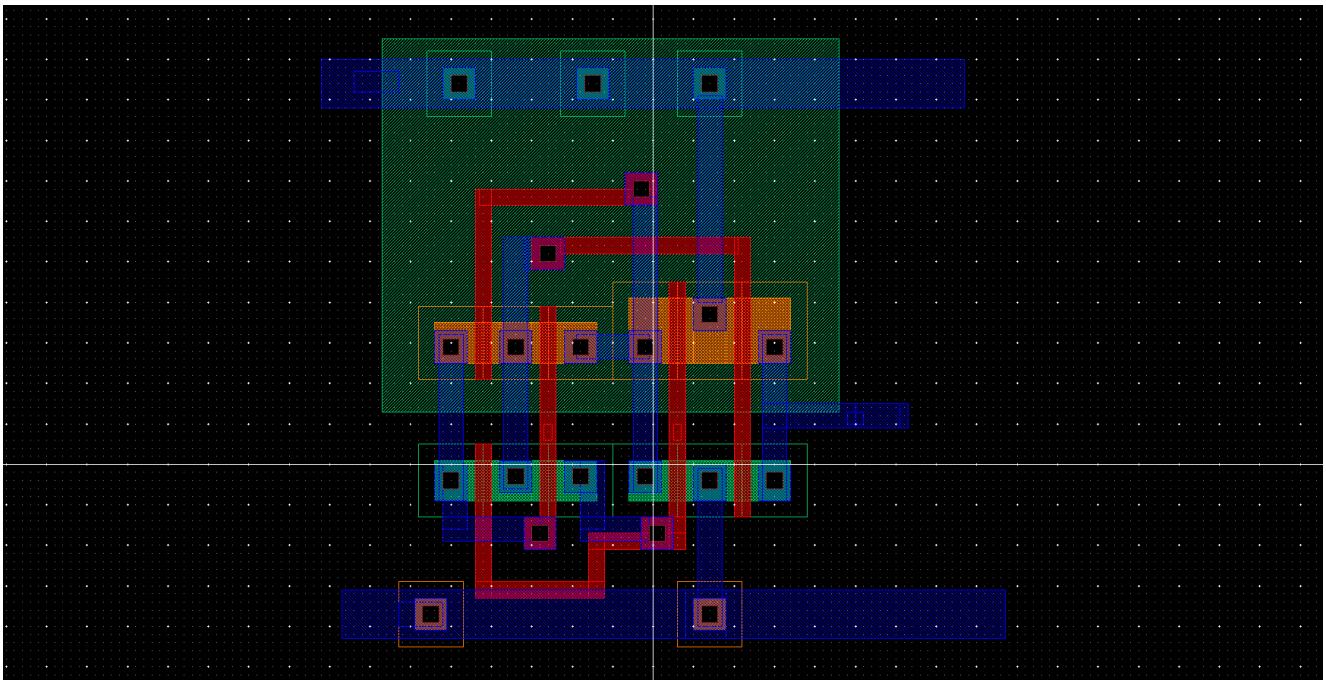
Layout of or8



Layout of xor2



Layout of xnor2



Part 10: Calculation for area of various cell block

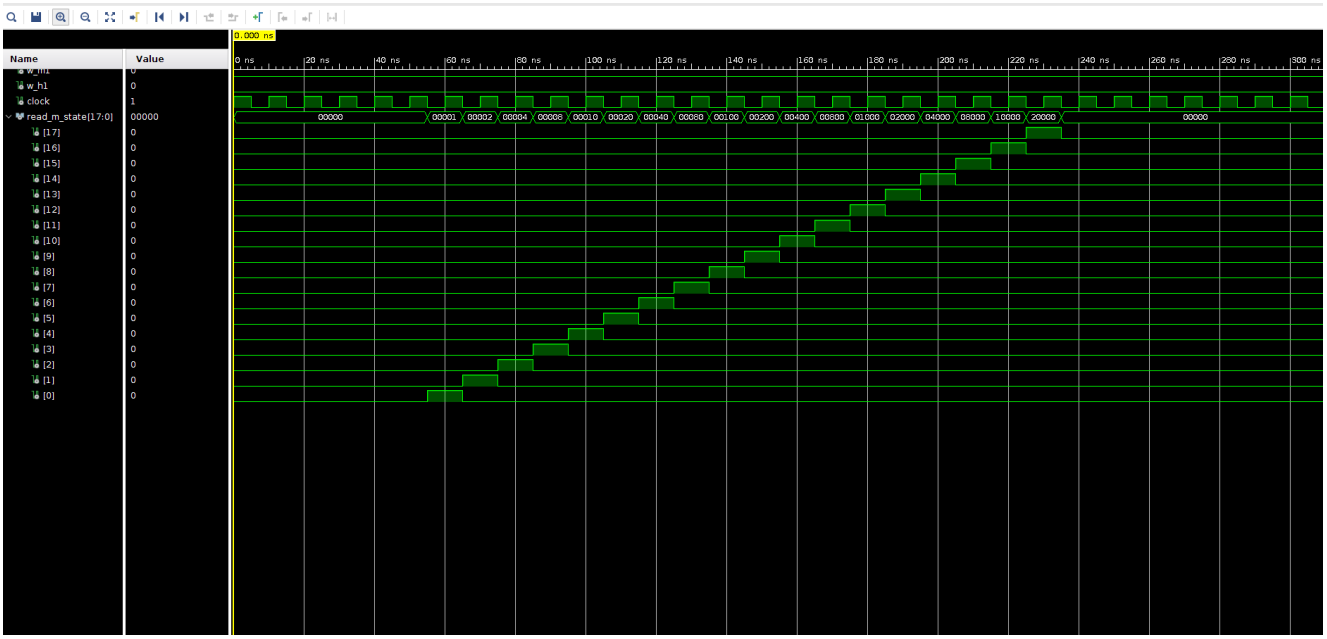
Cell name	Length(µm)	Width(µm)	Area(µm^2)
and2	22.05	9.6	211.68
and3	22.05	21.9	482.895
buff	22.05	12	264.6
busy	22.05	69.9	1541.295
cache	631.59	549	346742.91
decoder 2 to 4	22.05	110.4	2434.32
decoder 3 to 8	41.4	117.6	4868.64
DFF	22.05	26.4	582.12
Cache_32_byte	806.4	549	442713.6
Cache_bit_cell	22.05	63	1389.15
Cache_block_cell	159.75	271.65	43396.0875
Cache_byte_cell	158.1	63	9960.3
Cache_64_byte_control	22.05	333	7342.65

cache_control_ block	22.05	133.5	2943.675
chip	894.75	1257.45	1125103.388
D'Latch	22.05	16.8	370.44
hit_miss	22.05	99.3	2189.565
inverter	22.05	4.8	105.84
LRU_cell	22.05	91.5	2017.575
Mux_2to1 (bit)	22.05	33.75	744.1875
Mux_2to1 (byte)	159	33.75	5366.25
nor2	22.05	7.2	158.76
nor3	22.05	16.8	370.44
or3	22.05	14.4	317.52
or8	22.05	31.2	687.96
r_m_control	22.05	158.85	3502.6425
register_8bit	22.05	146.4	3228.12
state_machine	26.4	159	4197.6
Tag_valid_ block	512	54.3	27801.6
Tag_valid_ block-cell	159	301.35	47914.65
Tristate_buffer	22.05	259.65	5725.2825

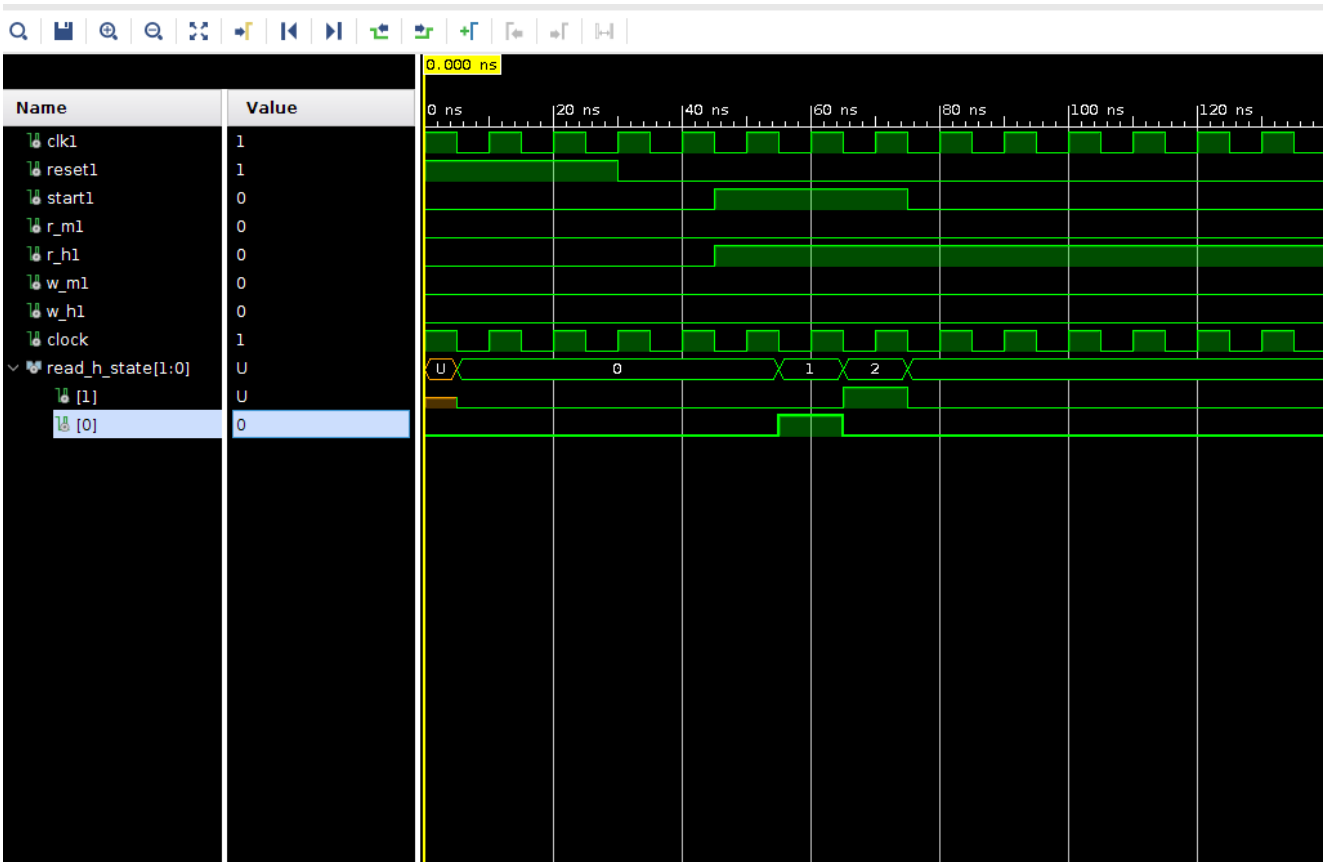
Tristate_buffer 8 bit	22.05	12	264.6
TX	159.1	12	1909.2
xnor2	22.05	4.95	109.1475
xor	22.05	21.6	476.28
Nand	22.05	14.4	317.52

Part 11: Performing Simulation

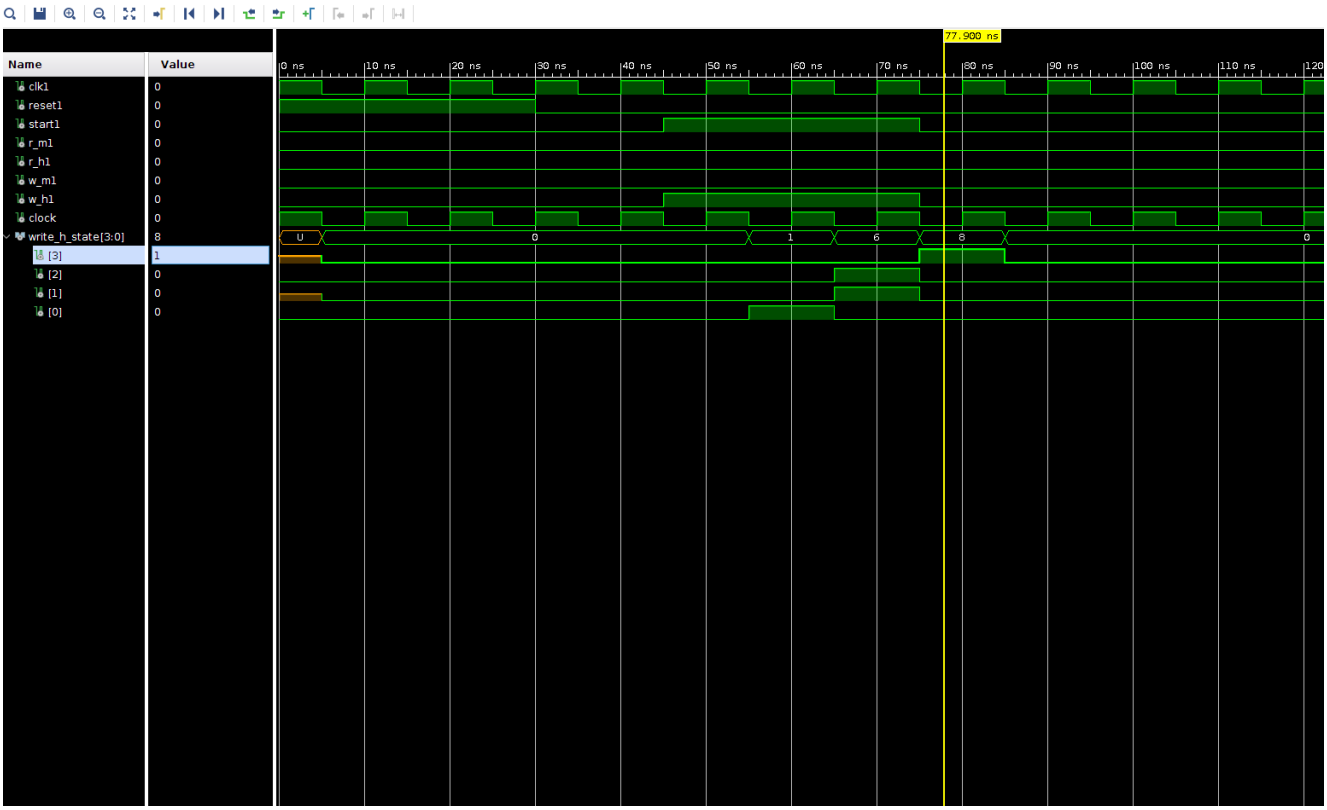
Flow of read miss in state machine:



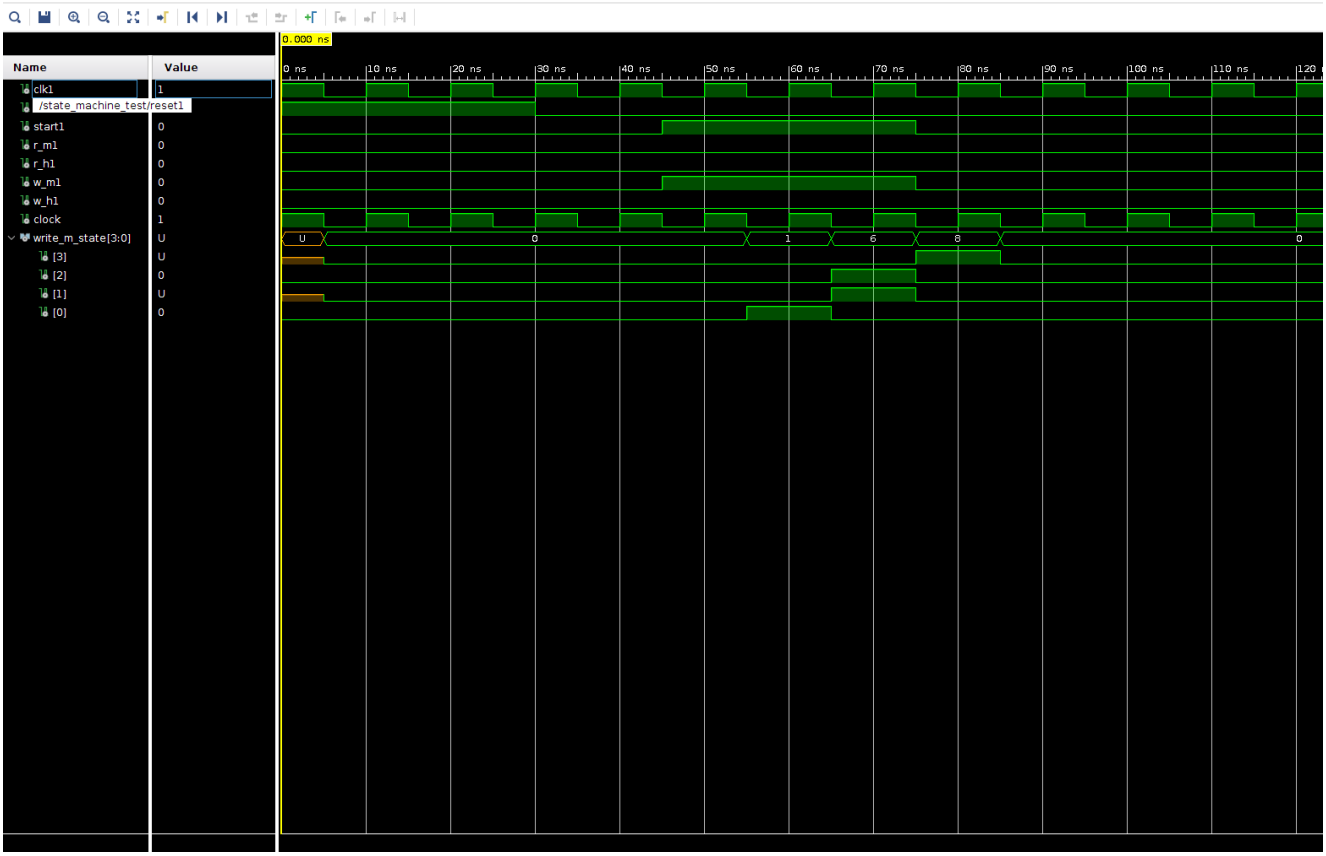
Flow of read hit in state machine:



Flow of write hit in state machine:

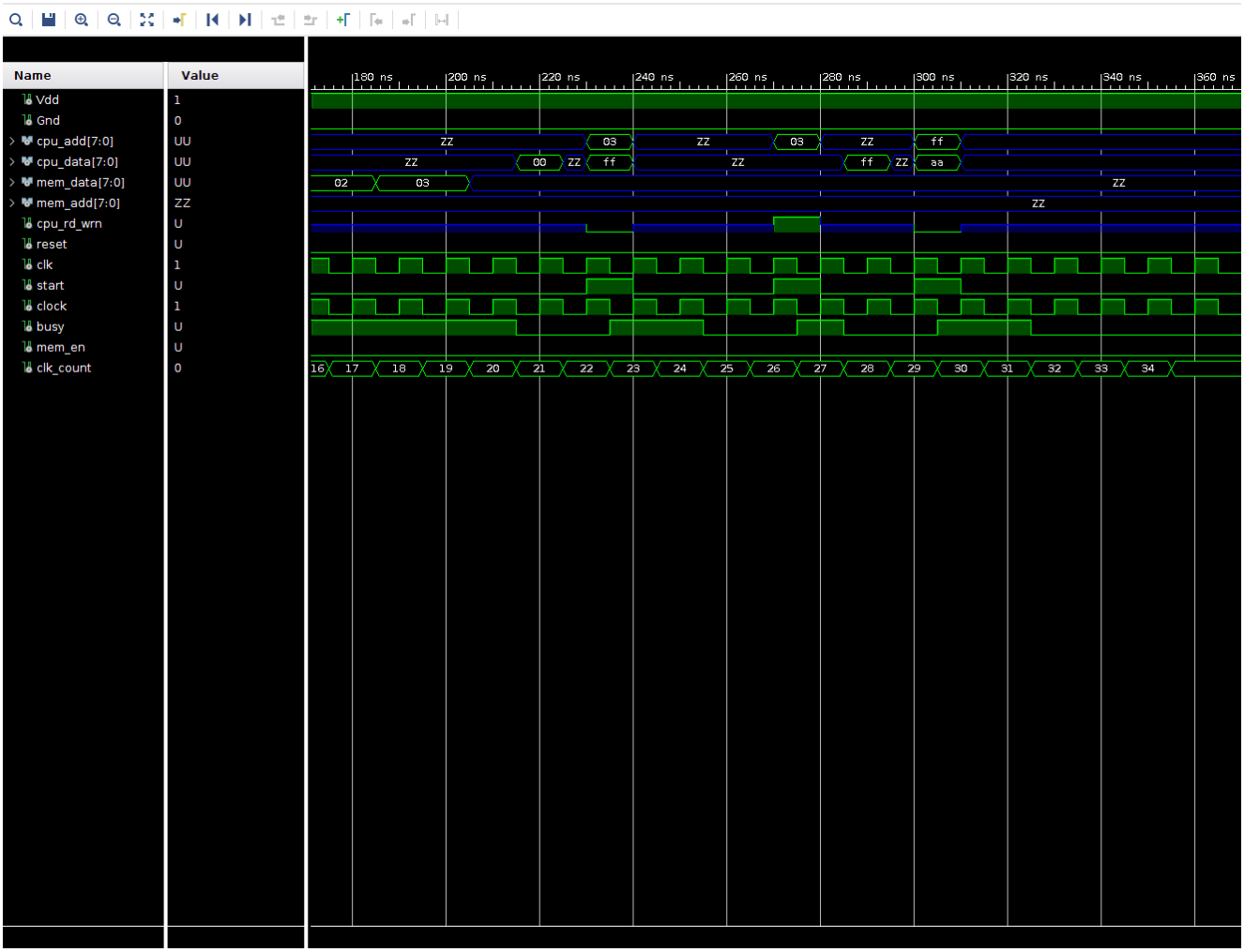


Flow of write miss in state machine:



Chip simulation (read miss state):

Chip simulation (read hit/write hit state):



Part 12: Code and LVS encrypted file

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity and2 is
 6: port(input1 : in std_logic;
 7:      input2 : in std_logic;
 8:      output : out std_logic);
 9: end and2;
10:
11: architecture structural of and2 is
12: begin
13:      output <= input2 and input1;
14: end structural;
15:
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity and3 is
 6: port(input1 : in std_logic;
 7:      input2 : in std_logic;
 8:      input3 : in std_logic;
 9:      output : out std_logic);
10: end and3;
11:
12: architecture structural of and3 is
13:
14: component and2
15: port(input1 : in std_logic;
16: input2 : in std_logic;
17: output : out std_logic);
18: end component;
19:
20: for and2_1, and2_2 : and2 use entity work.and2(structural);
21:
22: signal temp: std_logic;
23:
24: begin
25: and2_1 : and2 port map(input1, input2, temp);
26: and2_2 : and2 port map(input3, temp, output);
27: end structural;
```

```
 1: library IEEE;
 2: use IEEE.STD_LOGIC_1164.ALL;
 3:
 4:
 5: entity buff is
 6: port(input : in std_logic;
 7: output : out std_logic);
 8: end buff;
 9:
10: architecture structural of buff is
11:
12: begin
13: output<= input;
14: end structural;
```

```
 1: library IEEE;
 2: use IEEE.STD_LOGIC_1164.ALL;
 3:
 4: entity busy_block is
 5: port(start,reset,state0_loop,state0_en,op_busy : in std_logic;
 6:      busy : out std_logic
 7:      );
 8: end busy_block;
 9:
10: architecture structural of busy_block is
11:
12: component and2
13: port(input1 : in std_logic;
14:      input2 : in std_logic;
15:      output : out std_logic);
16: end component;
17:
18: component nor2
19: port(input1 : in std_logic;
20:      input2 : in std_logic;
21:      output : out std_logic);
22: end component;
23:
24: component or2
25: port(
26:     input1    : in  std_logic;
27:     input2 : in std_logic;
28:     output   : out std_logic);
29: end component;
30:
31: for and2_1 : and2 use entity work.and2(structural);
32: for nor2_1 : nor2 use entity work.nor2(structural);
33: for or2_1,or2_2,or2_3 : or2 use entity work.or2(structural);
34:
35: signal temp1,temp2,temp3,temp4 : std_logic;
36:
37: begin
38:
39: and2_1 : and2 port map(start, state0_en, temp1);
40: or2_1 : or2 port map(start,op_busy, temp2);
41: or2_2 : or2 port map(reset,state0_loop,temp3);
42: nor2_1 : nor2 port map(temp2, temp3,temp4);
43: or2_3 : or2 port map(temp1,temp4,busy);
44:
45: end structural;
```

```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity cache is
    6: port ( w_data :  in std_logic_vector(7 downto 0);
    7:        byte_en:in std_logic_vector(3 downto 0);
    8:        block_en: in std_logic_vector(7 downto 0);
    9:        rw_en : in std_logic;
   10:        r_data : out std_logic_vector(7 downto 0));
   11: end cache;
   12:
   13: architecture structural of cache is
   14:
   15: component cache_block_cell
   16: port (  w_data :  in std_logic_vector(7 downto 0);
   17:        byte_en :in std_logic_vector(3 downto 0);
   18:        block_en : in std_logic;
   19:        rw_en : in std_logic;
   20:        r_data : out std_logic_vector(7 downto 0));
   21: end component;
   22:
   23: for all : cache_block_cell use entity work.cache_block_cell(structural);
   24:
   25: begin
   26:
   27: cache_block_cell_0 : cache_block_cell port map(w_data, byte_en,block_en(0),rw_
en,r_data);
   28: cache_block_cell_1 : cache_block_cell port map(w_data, byte_en,block_en(1),rw_
en,r_data);
   29: cache_block_cell_2 : cache_block_cell port map(w_data, byte_en,block_en(2),rw_
en,r_data);
   30: cache_block_cell_3 : cache_block_cell port map(w_data, byte_en,block_en(3),rw_
en,r_data);
   31: cache_block_cell_4 : cache_block_cell port map(w_data, byte_en,block_en(4),rw_
en,r_data);
   32: cache_block_cell_5 : cache_block_cell port map(w_data, byte_en,block_en(5),rw_
en,r_data);
   33: cache_block_cell_6 : cache_block_cell port map(w_data, byte_en,block_en(6),rw_
en,r_data);
   34: cache_block_cell_7 : cache_block_cell port map(w_data, byte_en,block_en(7),rw_
en,r_data);
   35:
   36: end structural;
```

```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity cache_32byte is
    6: port ( m_data,c_data, CA_data,block_en :  in std_logic_vector(7 downto 0);
    7:        reset,CPU_rw_signal,w_cache,read_h_en, write_h_en,read_m_en,read_m, cac
he_en,s0,s1: in std_logic;
    8:        hm_signal : out std_logic;
    9:        r_data : out std_logic_vector(7 downto 0));
   10: end cache_32byte;
   11:
   12: architecture structural of cache_32byte is
   13:
   14: component cache
   15: port (  w_data :  in std_logic_vector(7 downto 0);
   16:        byte_en:in std_logic_vector(3 downto 0);
   17:        block_en: in std_logic_vector(7 downto 0);
   18:        rw_en : in std_logic;
   19:        r_data : out std_logic_vector(7 downto 0));
   20: end component;
   21:
   22: component tag_valid_block
   23: Port ( block_en : in std_logic_vector(7 downto 0);
   24:        reset,cache_tag_rw : in std_logic;
   25:        CA_reg : in std_logic_vector(2 downto 0);
   26:        tag_valid_data : out std_logic_vector(3 downto 0));
   27: end component;
   28:
   29: component cache_control_block
   30: port(CPU_rw_signal,w_cache,read_h_en, write_h_en,read_m_en, cache_en: in std_l
ogic;
   31:       cache_rw,cache_tag_rw:out std_logic);
   32: end component;
   33:
   34: component mux_2to1_byte
   35: port ( A  : in  std_logic_vector(7 downto 0);
   36:        B  : in  std_logic_vector(7 downto 0);
   37:        sel: in  std_logic;
   38:  output   : out std_logic_vector(7 downto 0));
   39: end component;
   40:
   41: component or2
   42: port ( input1  : in  std_logic;
   43:        input2  : in  std_logic;
   44:       output   : out std_logic);
   45: end component;
   46:
   47: component decoder_2to4
   48: port(input1,input2,en : in std_logic;
   49: output : out std_logic_vector(3 downto 0));
   50: end component;
   51:
   52: component mux_2to1_bit
   53:  port( A  : in  std_logic;
   54:        B  : in  std_logic;
   55:        sel: in  std_logic;
   56:        output   : out std_logic);
   57: end component;
   58:
   59: component hit_miss
   60:   port (
   61:     tag_valid_data   : in  std_logic_vector(3 downto 0);
   62:     CA_data   : in  std_logic_vector(2 downto 0);
   63:     reset : in std_logic;
   64:     hm_signal : out std_logic);
   65: end component;
   66:
   67: for all: mux_2to1_byte use entity work.mux_2to1_byte(structural);
   68: for all: mux_2to1_bit use entity work.mux_2to1_bit(structural);
   69: for all: decoder_2to4 use entity work.decoder_2to4(structural);
   70: for all: cache_control_block use entity work.cache_control_block(structural);
   71: for all: tag_valid_block use entity work.tag_valid_block(structural);
   72: for all: hit_miss use entity work.hit_miss(structural);
   73: for all: cache use entity work.cache(structural);
   74: signal w_data1 : std_logic_vector(7 downto 0);
   75: signal byte_en,tag_valid_data: std_logic_vector(3 downto 0);
   76: signal mux_byte_en,dec_s0,dec_s1,cache_rw,cache_tag_rw: std_logic;
   77: begin
   78: or2_1: or2 port map(w_cache, read_m, mux_byte_en);
   79: mux_2to1_byte_1: mux_2to1_byte port map(c_data,m_data,mux_byte_en,w_data1);
   80: mux_2to1_bit_1: mux_2to1_bit port map(CA_data(0),s0,w_cache,dec_s0);
   81: mux_2to1_bit_2: mux_2to1_bit port map(CA_data(1),s1,w_cache,dec_s1);
   82: decoder_2to4_1: decoder_2to4 port map(dec_s0,dec_s1,cache_tag_rw,byte_en);
   83: cache_control_block_1: cache_control_block port map(CPU_rw_signal,w_cache,read
_h_en, write_h_en,read_m_en, cache_en,cache_rw,cache_tag_rw);
   84: tag_valid_block_1: tag_valid_block port map(block_en,reset,cache_tag_rw, CA_da
ta(7 downto 5),tag_valid_data);
   85: hit_miss_1: hit_miss port map(tag_valid_data,CA_data(7 downto 5),reset,hm_sign
al);
   86: cache_1: cache port map(w_data1,byte_en,block_en,cache_rw,r_data);
   87: end structural;
```

```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity cache_bit_cell is
    6: port ( w_data :  in std_logic;
    7:        bit_en : in std_logic;
    8:        rw_en : in std_logic;
    9:        r_data : out std_logic);
   10: end cache_bit_cell;
   11:
   12: architecture structural of cache_bit_cell is
   13:
   14: component Dlatch
   15: port (   d   : in  std_logic;
   16:          clk : in  std_logic;
   17:          q   : out std_logic);
   18: end component;
   19:
   20: component tristate_buffer
   21: port (   input : in std_logic;
   22:              en : in std_logic;
   23:          output:out std_logic);
   24: end component;
   25:
   26: component and2
   27: port(input1 : in std_logic;
   28:      input2 : in std_logic;
   29:      output : out std_logic);
   30: end component;
   31:
   32: component inverter
   33: port (
   34:     input    : in  std_logic;
   35:     output   : out std_logic);
   36: end component;
   37:
   38:
   39: for Dlatch_1 : Dlatch use entity work.Dlatch(structural);
   40: for tristate_buffer_1 : tristate_buffer use entity work.tristate_buffer(struct
ural);
   41: for inv_1 : inverter use entity work.inverter(structural);
   42: for and2_1, and2_2 : and2 use entity work.and2(structural);
   43:
   44: signal rw_enb, en, clk, q: std_logic;
   45:
   46: begin
   47: inv_1 : inverter port map(rw_en, rw_enb);
   48: and2_1 : and2 port map(rw_en, bit_en, en);
   49: and2_2 : and2 port map(rw_enb, bit_en, clk);
   50: Dlatch_1 : Dlatch port map(w_data, clk, q);
   51: tristate_buffer_1 : tristate_buffer port map(q,en,r_data);
   52: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity cache_block_cell is
 6: port ( w_data :  in std_logic_vector(7 downto 0);
 7:        byte_en:in std_logic_vector(3 downto 0);
 8:        block_en : in std_logic;
 9:        rw_en : in std_logic;
10:        r_data : out std_logic_vector(7 downto 0));
11: end cache_block_cell;
12:
13: architecture structural of cache_block_cell is
14:
15: component cache_byte_cell
16: port ( w_data :  in std_logic_vector(7 downto 0);
17:        byte_en : in std_logic;
18:        rw_en : in std_logic;
19:        r_data : out std_logic_vector(7 downto 0));
20: end component;
21:
22: component and2
23: port(input1 : in std_logic;
24:      input2 : in std_logic;
25:      output : out std_logic);
26: end component;
27:
28: for all : and2 use entity work.and2(structural);
29: for all : cache_byte_cell use entity work.cache_byte_cell(structural);
30:
31: signal by_0,by_1,by_2,by_3: std_logic;
32: begin
33:
34: and2_1 : and2 port map(byte_en(0), block_en, by_0);
35: and2_2 : and2 port map(byte_en(1), block_en, by_1);
36: and2_3 : and2 port map(byte_en(2), block_en, by_2);
37: and2_4 : and2 port map(byte_en(3), block_en, by_3);
38:
39: cache_byte_cell_1 : cache_byte_cell port map(w_data,by_0,rw_en,r_data);
40: cache_byte_cell_2 : cache_byte_cell port map(w_data,by_1,rw_en,r_data);
41: cache_byte_cell_3 : cache_byte_cell port map(w_data,by_2,rw_en,r_data);
42: cache_byte_cell_4 : cache_byte_cell port map(w_data,by_3,rw_en,r_data);
43:
44: end structural;
```

```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity cache_byte_cell is
    6: port ( w_data :  in std_logic_vector(7 downto 0);
    7:        byte_en : in std_logic;
    8:        rw_en : in std_logic;
    9:        r_data : out std_logic_vector(7 downto 0));
   10: end cache_byte_cell;
   11:
   12: architecture structural of cache_byte_cell is
   13:
   14: component cache_bit_cell
   15: port ( w_data :  in std_logic;
   16:        bit_en : in std_logic;
   17:        rw_en : in std_logic;
   18:        r_data : out std_logic);
   19: end component;
   20:
   21: for cache_bit_cell_0, cache_bit_cell_1,cache_bit_cell_2,cache_bit_cell_3,cache
_bit_cell_4, cache_bit_cell_5, cache_bit_cell_6, cache_bit_cell_7: cache_bit_cell use
entity work.cache_bit_cell(structural);
   22:
   23: begin
   24:
   25: cache_bit_cell_0 : cache_bit_cell port map(w_data(0),byte_en,rw_en,r_data(0));
   26: cache_bit_cell_1 : cache_bit_cell port map(w_data(1),byte_en,rw_en,r_data(1));
   27: cache_bit_cell_2 : cache_bit_cell port map(w_data(2),byte_en,rw_en,r_data(2));
   28: cache_bit_cell_3 : cache_bit_cell port map(w_data(3),byte_en,rw_en,r_data(3));
   29: cache_bit_cell_4 : cache_bit_cell port map(w_data(4),byte_en,rw_en,r_data(4));
   30: cache_bit_cell_5 : cache_bit_cell port map(w_data(5),byte_en,rw_en,r_data(5));
   31: cache_bit_cell_6 : cache_bit_cell port map(w_data(6),byte_en,rw_en,r_data(6));
   32: cache_bit_cell_7 : cache_bit_cell port map(w_data(7),byte_en,rw_en,r_data(7));
   33:
   34: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity cache_control_64_byte is
 6:   port (
 7:   C_rw,state0_en,hm_signal0, hm_signal1,LRU_signal : in std_logic;
 8:     read_h,write_h,read_m,write_m,cache0_en, cache1_en : out std_logic);
 9: end cache_control_64_byte;
10:
11: architecture structural of cache_control_64_byte is
12:
13: component or2
14:   port (
15:   input1   : in  std_logic;
16:   input2   : in  std_logic;
17:   output : out std_logic);
18: end component;
19:
20: component and2
21:   port (
22:   input1   : in  std_logic;
23:   input2   : in  std_logic;
24:   output : out std_logic);
25: end component;
26:
27: component decoder_2to4
28: port(input1,input2,en : in std_logic;
29: output : out std_logic_vector(3 downto 0));
30: end component;
31:
32: component buff
33: port(input : in std_logic;
34: output : out std_logic);
35: end component;
36:
37: component inverter
38: port(input : in std_logic;
39: output : out std_logic);
40: end component;
41:
42: component or3
43: port(input1 : in std_logic;
44:      input2 : in std_logic;
45:      input3 : in std_logic;
46:      output : out std_logic);
47: end component;
48:
49: for all : or2 use entity work.or2(structural);
50: for all : or3 use entity work.or3(structural);
51: for all : and2 use entity work.and2(structural);
52: for all : decoder_2to4 use entity work.decoder_2to4(structural);
53: for all : buff use entity work.buff(structural);
54: for all : inverter use entity work.inverter(structural);
55:
56:
57: signal hm_signal,LRU_signal_b: std_logic;
58: signal temp: std_logic_vector(3 downto 0);
59: signal cache0,cache1: std_logic_vector(2 downto 0);
60:
61: begin
62: inv_1: inverter port map(LRU_signal,LRU_signal_b);
63: or2_1 :  or2 port map(hm_signal0, hm_signal1, hm_signal);
64: decoder_2to4_1 : decoder_2to4 port map(input1=>hm_signal, input2=>C_rw, en=>st
ate0_en,output=>temp);
65: buff_1: buff port map(temp(0),write_m);
66: buff_2: buff port map(temp(1),write_h);
67: buff_3: buff port map(temp(2),read_m);
68: buff_4: buff port map(temp(3),read_h);
69: and2_1 :  and2 port map(hm_signal0, temp(1), cache0(0));
70: and2_2 :  and2 port map( LRU_signal_b, temp(2), cache0(1));
71: and2_3 :  and2 port map(hm_signal0, temp(3), cache0(2));
72:
73: and2_4 :  and2 port map(hm_signal1, temp(1), cache1(0));
74: and2_5 :  and2 port map(LRU_signal, temp(2), cache1(1));
75: and2_6 :  and2 port map(hm_signal1, temp(3), cache1(2));
76: or3_1 :  or3 port map(cache0(0),cache0(1),cache0(2),cache0_en);
77: or3_2 :  or3 port map(cache1(0),cache1(1),cache1(2),cache1_en);
78:
79:
80:
81: end structural;
82:
```

```
    1:
    2: library IEEE;
    3: use IEEE.STD_LOGIC_1164.ALL;
    4:
    5: entity cache_control_block is
    6: port(CPU_rw_signal,w_cache,read_h_en, write_h_en,read_m_en, cache_en: in std_l
ogic;
    7:       cache_rw,cache_tag_rw:out std_logic);
    8: end cache_control_block;
    9:
   10: architecture structural of cache_control_block is
   11:
   12:
   13: component inverter
   14:  port (
   15:     input    : in  std_logic;
   16:     output   : out std_logic);
   17: end component;
   18:
   19: component or2
   20: port(
   21:     input1    : in  std_logic;
   22:     input2 : in std_logic;
   23:     output   : out std_logic);
   24: end component;
   25:
   26: component and2
   27: port(
   28:     input1    : in  std_logic;
   29:     input2 : in std_logic;
   30:     output   : out std_logic);
   31: end component;
   32:
   33: for all : inverter use entity work.inverter(structural);
   34: for all : or2 use entity work.or2(structural);
   35: for all : and2 use entity work.and2(structural);
   36:
   37: signal w_cache_b,temp1,temp2 : std_logic;
   38: signal CPU_rw_signal1,w_cache1,read_h_en1, write_h_en1,read_m_en1: std_logic;
   39:
   40:
   41: begin
   42: and2_1: and2 port map(CPU_rw_signal,cache_en,CPU_rw_signal1);
   43: and2_2: and2 port map(w_cache,cache_en,w_cache1);
   44: and2_3: and2 port map(read_h_en,cache_en,read_h_en1);
   45: and2_4: and2 port map(write_h_en,cache_en,write_h_en1);
   46: and2_5: and2 port map(read_m_en,cache_en,read_m_en1);
   47: inv_1 : inverter port map(w_cache1,w_cache_b);
   48: or2_1 :or2 port map(CPU_rw_signal1,w_cache_b,cache_rw);
   49: or2_2 : or2 port map(w_cache1,read_m_en1,temp1);
   50: or2_3 : or2 port map(temp1,write_h_en1,temp2);
   51: or2_4 : or2 port map(read_h_en1,temp2,cache_tag_rw);
   52:
   53: end structural;
```

```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity chip is
    6: port (
    7:       cpu_add    : in  std_logic_vector(7 downto 0);
    8:       cpu_data   : inout  std_logic_vector(7 downto 0);
    9:       cpu_rd_wrn : in  std_logic;
   10:       start      : in  std_logic;
   11:       clk        : in  std_logic;
   12:       reset      : in  std_logic;
   13:       mem_data   : in  std_logic_vector(7 downto 0);
   14:       Vdd          : in  std_logic;
   15:       Gnd        : in  std_logic;
   16:       busy       : out std_logic;
   17:       mem_en     : out std_logic;
   18:       mem_add    : out std_logic_vector(7 downto 0));
   19: end chip;
   20:
   21: architecture structural of chip is
   22:
   23: component cache_32byte
   24: port ( m_data,c_data, CA_data,block_en :  in std_logic_vector(7 downto 0);
   25:        reset,CPU_rw_signal,w_cache,read_h_en, write_h_en,read_m_en,read_m, cac
he_en,s0,s1: in std_logic;
   26:        hm_signal : out std_logic;
   27:        r_data : out std_logic_vector(7 downto 0));
   28: end component;
   29:
   30: component register_8bit
   31:   port ( d   : in  std_logic_vector(7 downto 0);
   32:          clk : in  std_logic;
   33:          q   : out std_logic_vector(7 downto 0));
   34: end component;
   35: component dff
   36:   port ( d   : in  std_logic;
   37:          clk : in  std_logic;
   38:          q   : out std_logic);
   39: end component;
   40:
   41: component decoder_3to8
   42: port(input1,input2, input3: in std_logic;
   43: output: out std_logic_vector(7 downto 0));
   44: end component;
   45:
   46: component inverter
   47:   port (
   48:     input    : in  std_logic;
   49:     output   : out std_logic);
   50: end component;
   51:
   52: component and2
   53: port(input1 : in std_logic;
   54:      input2 : in std_logic;
   55:      output : out std_logic);
   56: end component;
   57:
   58: component nor2
   59: port(input1 : in std_logic;
   60:      input2 : in std_logic;
   61:      output : out std_logic);
   62: end component;
   63:
   64: component or2
   65: port(input1 : in std_logic;
   66:      input2 : in std_logic;
   67:      output : out std_logic);
   68: end component;
   69:
   70: component buff
   71:   port (
   72:     input    : in  std_logic;
   73:     output   : out std_logic);
   74: end component;
   75:
   76: component LRU_cell
   77: port ( reset, read_m_en :  in std_logic;
   78:        LRU_signal : out std_logic);
   79: end component;
   80:
   81: component cache_control_64_byte
   82:   port (
   83:   C_rw,state0_en,hm_signal0, hm_signal1,LRU_signal : in std_logic;
   84:     read_h,write_h,read_m,write_m,cache0_en, cache1_en : out std_logic);
   85: end component;
   86:
   87: component state_machine
   88: port(clk, reset, start, read_m,read_h,write_m,write_h : in std_logic;
   89: state0_en,state0_loop,read_h_en,write_h_en,read_m_en,memory_en,read_en,op_busy
 : out std_logic;
   90: data_receive: out std_logic_vector(7 downto 0));
   91: end component;
   92:
   93: component r_m_control
   94: port(input: in std_logic_vector(7 downto 0);
   95:      s0,s1,w_cache : out std_logic
   96:      );
   97: end component;
   98:
   99: component busy_block
  100: port(start,reset,state0_loop,state0_en,op_busy : in std_logic;
  101:      busy : out std_logic
  102:      );
  103: end component;
  104:
  105: component tristate_buffer_8bit
  106:
  107:   Port ( input    : in  STD_LOGIC_VECTOR(7 downto 0);
  108:          en   : in  STD_LOGIC;
  109:          output    : out STD_LOGIC_VECTOR(7 downto 0));
  110: end component;
  111:
  112: component or8
  113: port(input1 : in std_logic_vector (7 downto 0);
  114:      input2 : in std_logic_vector (7 downto 0);
  115:      output : out std_logic_vector (7 downto 0));
  116: end component;
  117:
  118:
  119: for all: register_8bit  use entity work.register_8bit(structural);
  120: for all : inverter use entity work.inverter(structural);
  121: for all : buff use entity work.buff(structural);
  122: for all: dff use entity work.dff(structural);
```

```
  123: for all: decoder_3to8 use entity work.decoder_3to8(structural);
  124: for all: cache_32byte use entity work.cache_32byte(structural);
  125: for all: LRU_cell  use entity work.LRU_cell(structural);
  126: for all: cache_control_64_byte  use entity work.cache_control_64_byte(structur
al);
  127: for all: state_machine  use entity work.state_machine(structural);
  128: for all: r_m_control use entity work.r_m_control(structural);
  129: for all: busy_block use entity work.busy_block(structural);
  130: for all: and2 use entity work.and2(structural);
  131: for all: nor2 use entity work.nor2(structural);
  132: for all: or2 use entity work.or2(structural);
  133: for all: tristate_buffer_8bit use entity work.tristate_buffer_8bit(structural)
;
  134: for all: or8 use entity work.or8(structural);
  135:
  136: signal start_b,CPU_rw_signal,w_cache,read_h_en, write_h_en,write_m_en,read_m_e
n, cache0_en,cache1_en,s0,s1,hm0_signal,hm1_signal,LRU_signal,state0_en,read_m,read_h,
write_m,write_h: std_logic;
  137: signal CA_data,CD_data,block_en,cache0_data,cache1_data,data_receive,r_data: s
td_logic_vector(7 downto 0);
  138: signal state0_loop,memory_en1, read_en,op_busy,temp1,temp2,temp3,temp4: std_lo
gic;
  139: begin
  140: inv_1 : inverter port map(start,start_b);
  141: cpu_add_reg: register_8bit port map(cpu_add,start_b,CA_data);
  142: cpu_data_reg: register_8bit port map(cpu_data,start_b,CD_data);
  143: cpu_rd_wrn_reg: dff port map(cpu_rd_wrn,start_b,CPU_rw_signal);
  144: block_add: decoder_3to8 port map(CA_data(2),CA_data(3),CA_data(4),block_en);
  145: cache_0:cache_32byte port map (mem_data,CD_data,CA_data,block_en,reset,CPU_rw_
signal,w_cache,read_h_en, write_h_en,read_m_en, read_en,cache0_en,s0,s1,hm0_signal,cac
he0_data);
  146: cache_1:cache_32byte port map (mem_data,CD_data,CA_data,block_en,reset,CPU_rw_
signal,w_cache,read_h_en, write_h_en,read_m_en, read_en,cache1_en,s0,s1,hm1_signal,cac
he1_data);
  147: LRU_block: LRU_cell port map(reset,read_m_en,LRU_signal);
  148: Control_block: cache_control_64_byte port map(CPU_rw_signal,state0_en,hm0_sign
al, hm1_signal,LRU_signal,read_h,write_h,read_m,write_m,cache0_en, cache1_en);
  149: State_Control: state_machine port map(clk, reset, start, read_m,read_h,write_m
,write_h,state0_en,state0_loop,read_h_en,write_h_en,read_m_en,memory_en1,read_en,op_bu
sy,data_receive);
  150: Memory_enable: buff port map(memory_en1,mem_en);
  151: Read_miss_control:r_m_control port map(data_receive,s0,s1,w_cache);
  152: BUSY_blk: busy_block port map(start,reset,state0_loop,state0_en,op_busy,busy);

  153: or2_1:or2 port map(CA_data(1),CA_data(0), temp1);
  154: nor2_1:nor2 port map(CA_data(1),CA_data(0), temp2);
  155: and2_1:and2 port map(temp1,temp2, temp3);
  156: Memory_address:tristate_buffer_8bit port map(input(7 downto 2)=>CA_data(7 down
to 2),input(1)=>temp3,input(0)=>temp3,en=>memory_en1, output=>mem_add);
  157: or8_1:or8 port map(cache0_data,cache1_data, r_data);
  158: or2_2:or2 port map(read_h_en,read_m_en, temp4);
  159: Cache_data:tristate_buffer_8bit port map( r_data,temp4,cpu_data);
  160: end structural;
```

```
  1: -- Entity: chip_full_test
  2: -- Architecture : test
  3: -- Author: cpatel2
  4: -- Created On: 11/01/05
  5: --
  6: library IEEE;
  7: use IEEE.std_logic_1164.all;
  8: use IEEE.std_logic_textio.all;
  9: use IEEE.std_logic_arith.all;
 10: use STD.textio.all;
 11:
 12: entity chip_full_test is
 13:
 14: end chip_full_test;
 15:
 16: architecture test of chip_full_test is
 17:
 18:   component chip
 19:     port (
 20:       cpu_add    : in  std_logic_vector(7 downto 0);
 21:       cpu_data   : inout  std_logic_vector(7 downto 0);
 22:       cpu_rd_wrn : in  std_logic;
 23:       start      : in  std_logic;
 24:       clk        : in  std_logic;
 25:       reset      : in  std_logic;
 26:       mem_data   : in  std_logic_vector(7 downto 0);
 27:       Vdd        : in  std_logic;
 28:       Gnd        : in  std_logic;
 29:       busy       : out std_logic;
 30:       mem_en     : out std_logic;
 31:       mem_add    : out std_logic_vector(7 downto 0));
 32:   end component;
 33:
 34:
 35:
 36:   for c1 : chip use entity work.chip(structural);
 37:
 38:   signal Vdd, Gnd: std_logic;
 39:   signal cpu_add, cpu_data, mem_data, mem_add: std_logic_vector(7 downto 0);
 40:   signal cpu_rd_wrn, reset, clk, start, clock, busy, mem_en: std_logic;
 41:
 42:   signal clk_count: integer:=0;
 43:
 44: procedure print_output is
 45:    variable out_line: line;
 46:
 47:    begin
 48:    write (out_line, string' (" Clock: "));
 49:    write (out_line, clk_count);
 50:    write (out_line, string'(" Start: "));
 51:    write (out_line, start);
 52:    write (out_line, string'(" Cpu Read/Write: "));
 53:    write (out_line, cpu_rd_wrn);
 54:    write (out_line, string'(" Reset: "));
 55:    write (out_line, reset);
 56:    writeline(output, out_line);
 57:
 58:    write (out_line, string' (" CPU address: "));
 59:    write (out_line, cpu_add);
 60:    write (out_line, string'(" CPU data: "));
 61:    write (out_line, cpu_data);
 62:    writeline(output, out_line);
 63:
 64:    write (out_line, string'(" Memory data: "));
 65:    write (out_line, mem_data);
 66:    writeline(output, out_line);
 67:    writeline(output, out_line);
 68:
 69:    write (out_line, string'(" Busy: "));
 70:    write (out_line, busy);
 71:    write (out_line, string'(" Memory  Enable: "));
 72:    write (out_line, mem_en);
 73:    writeline(output, out_line);
 74:
 75:    write (out_line, string'(" Memory  Address: "));
 76:    write (out_line, mem_add);
 77:    writeline(output, out_line);
 78:
 79:    write (out_line, string'(" ----------------------------------------------")
);
 80:    writeline(output, out_line);
 81:
 82:
 83: end print_output;
 84:
 85:
 86:
 87: begin
 88:
 89:   Vdd <= '1';
 90:   Gnd <= '0';
 91:   clk <= clock;
 92:
 93:   c1 : chip port map (cpu_add, cpu_data, cpu_rd_wrn, start, clk, reset, mem_da
ta, Vdd, Gnd, busy, mem_en, mem_add);
 94:
 95:   clking : process
 96:   begin
 97:     clock<= '1', '0' after 5 ns;
 98:     wait for 10 ns;
 99:   end process clking;
100:
101:   io_process: process
102:
103:     file infile  : text is in "./chip_full_in.txt";
104:     variable buf: line;
105:     variable value: std_logic_vector(7 downto 0);
106:     variable value1: std_logic;
107:
108:   begin
109:
110:     while not (endfile(infile)) loop
111:
112:       wait until rising_edge(clock);
113:
114:       readline(infile, buf);
115:
116:       readline(infile, buf);
117:       read(buf, value);
118:       cpu_add <= value;
119:
120:       readline(infile, buf);
121:       read(buf, value);
122:       cpu_data <= value;
```

```
  123:
  124:       readline(infile, buf);
  125:       read(buf, value1);
  126:       cpu_rd_wrn <= value1;
  127:
  128:       readline(infile, buf);
  129:       read(buf, value1);
  130:       start <= value1;
  131:
  132:       readline(infile, buf);
  133:       read(buf, value1);
  134:       reset <= value1;
  135:
  136:       clk_count <= clk_count+1;
  137:
  138:       wait until falling_edge(clock);
  139:
  140:       readline(infile, buf);
  141:       read(buf, value);
  142:       mem_data <= value;
  143:
  144:     end loop;
  145:     wait;
  146:
  147:   end process io_process;
  148:
  149: print_process: process
  150:
  151:   variable out_line: line;
  152:
  153: begin
  154:
  155:   wait until ((falling_edge(clock) and start ='1') or busy'EVENT or mem_en'EVE
NT);
  156:   wait for 1 ns;
  157:   print_output;
  158:
  159: end process print_process;
  160:
  161: end test;
```

```
  1: -- Entity: chip_test
  2: -- Architecture : test
  3: -- Author: cpatel2
  4: -- Created On: 11/01/05
  5: --
  6: library IEEE;
  7: use IEEE.std_logic_1164.all;
  8: use IEEE.std_logic_textio.all;
  9: use IEEE.std_logic_arith.all;
 10: use STD.textio.all;
 11:
 12: entity chip_test is
 13:
 14: end chip_test;
 15:
 16: architecture test of chip_test is
 17:
 18:   component chip
 19:     port (
 20:       cpu_add    : in  std_logic_vector(7 downto 0);
 21:       cpu_data   : inout  std_logic_vector(7 downto 0);
 22:       cpu_rd_wrn : in  std_logic;
 23:       start      : in  std_logic;
 24:       clk        : in  std_logic;
 25:       reset      : in  std_logic;
 26:       mem_data   : in  std_logic_vector(7 downto 0);
 27:       Vdd        : in  std_logic;
 28:       Gnd        : in  std_logic;
 29:       busy       : out std_logic;
 30:       mem_en     : out std_logic;
 31:       mem_add    : out std_logic_vector(7 downto 0));
 32:   end component;
 33:
 34:
 35:
 36:   for c1 : chip use entity work.chip(structural);
 37:
 38:   signal Vdd, Gnd: std_logic;
 39:   signal cpu_add, cpu_data, mem_data, mem_add: std_logic_vector(7 downto 0);
 40:   signal cpu_rd_wrn, reset, clk, start, clock, busy, mem_en: std_logic;
 41:
 42:   signal clk_count: integer:=0;
 43:
 44: procedure print_output is
 45:    variable out_line: line;
 46:
 47:    begin
 48:    write (out_line, string' (" Clock: "));
 49:    write (out_line, clk_count);
 50:    write (out_line, string'(" Start: "));
 51:    write (out_line, start);
 52:    write (out_line, string'(" Cpu Read/Write: "));
 53:    write (out_line, cpu_rd_wrn);
 54:    write (out_line, string'(" Reset: "));
 55:    write (out_line, reset);
 56:    writeline(output, out_line);
 57:
 58:    write (out_line, string' (" CPU address: "));
 59:    write (out_line, cpu_add);
 60:    write (out_line, string'(" CPU data: "));
 61:    write (out_line, cpu_data);
 62:    writeline(output, out_line);
 63:
 64:    write (out_line, string'(" Memory data: "));
 65:    write (out_line, mem_data);
 66:    writeline(output, out_line);
 67:    writeline(output, out_line);
 68:
 69:    write (out_line, string'(" Busy: "));
 70:    write (out_line, busy);
 71:    write (out_line, string'(" Memory  Enable: "));
 72:    write (out_line, mem_en);
 73:    writeline(output, out_line);
 74:
 75:    write (out_line, string'(" Memory  Address: "));
 76:    write (out_line, mem_add);
 77:    writeline(output, out_line);
 78:
 79:    write (out_line, string'(" ------------------------------------------")
);
 80:    writeline(output, out_line);
 81:
 82:
 83: end print_output;
 84:
 85:
 86:
 87: begin
 88:
 89:   Vdd <= '1';
 90:   Gnd <= '0';
 91:   clk <= clock;
 92:
 93:   c1 : chip port map (cpu_add, cpu_data, cpu_rd_wrn, start, clk, reset, mem_da
ta, Vdd, Gnd, busy, mem_en, mem_add);
 94:
 95:   clking : process
 96:   begin
 97:     clock<= '1', '0' after 5 ns;
 98:     wait for 10 ns;
 99:   end process clking;
100:
101:   io_process: process
102:
103:     file infile  : text is in "./chip_in.txt";
104:     variable out_line: line;
105:     variable buf: line;
106:     variable value: std_logic_vector(7 downto 0);
107:     variable value1: std_logic;
108:
109:   begin
110:
111:     while not (endfile(infile)) loop
112:
113:       wait until rising_edge(clock);
114:       print_output;
115:
116:       readline(infile, buf);
117:       read(buf, value);
118:       cpu_add <= value;
119:
120:       readline(infile, buf);
121:       read(buf, value);
122:       cpu_data <= value;
```

```
123:
124:       readline(infile, buf);
125:       read(buf, value1);
126:       cpu_rd_wrn <= value1;
127:
128:       readline(infile, buf);
129:       read(buf, value1);
130:       start <= value1;
131:
132:       readline(infile, buf);
133:       read(buf, value1);
134:       reset <= value1;
135:
136:       wait until falling_edge(clock);
137:
138:       readline(infile, buf);
139:       read(buf, value);
140:       mem_data <= value;
141:
142:       clk_count <= clk_count+1;
143:
144:       print_output;
145:
146:     end loop;
147:     wait;
148:
149:   end process io_process;
150:
151:
152: end test;
```

```
    1: library STD;
    2: library IEEE;
    3: use IEEE.STD_LOGIC_1164.ALL;
    4:
    5:
    6: entity decoder_2to4 is
    7: port(input1,input2,en : in std_logic;
    8: output : out std_logic_vector(3 downto 0));
    9: end decoder_2to4;
   10:
   11: architecture structural of decoder_2to4 is
   12:
   13: component inverter
   14: port(input : in std_logic;
   15:      output : out std_logic);
   16: end component;
   17:
   18: component and3
   19: port(input1 : in std_logic;
   20:      input2 : in std_logic;
   21:      input3 : in std_logic;
   22:      output : out std_logic);
   23: end component;
   24:
   25:
   26: for inv_1,inv_2 : inverter use entity work.inverter(structural);
   27: for and3_1, and3_2, and3_3, and3_4 : and3 use entity work.and3(structural);
   28:
   29: signal input1_b, input2_b : std_logic;
   30:
   31: begin
   32:
   33: inv_1 : inverter port map(input=>input1, output=>input1_b);
   34: inv_2 : inverter port map(input=>input2, output=>input2_b);
   35:
   36: and3_1 : and3 port map(input1=>input2_b, input2=>input1_b, input3=>en, output=
>output(0));
   37: and3_2 : and3 port map(input1=>input2_b, input2=>input1, input3=>en, output=>o
utput(1));
   38: and3_3 : and3 port map(input1=>input2, input2=>input1_b,input3=> en,output=> o
utput(2));
   39: and3_4 : and3 port map(input1=>input2, input2=>input1, input3=>en, output=>out
put(3));
   40:
   41: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4: use IEEE.std_logic_textio.all;
 5: use STD.textio.all;
 6:
 7: entity decoder_2to4_test is
 8:
 9: end decoder_2to4_test;
10:
11: architecture test of decoder_2to4_test is
12:
13: component decoder_2to4
14: port(input1,input2,en : in std_logic;
15: output : out std_logic_vector(3 downto 0));
16: end component;
17:
18: for decoder_2to4_1: decoder_2to4 use entity work.decoder_2to4structural);
19: signal s01,s11,en1: std_logic;
20: signal y: std_logic_vector(3 downto 0);
21:
22:
23: begin
24:
25: decoder_2to4_1 : decoder_2to4 port map (s01,s11,en1,y);
26:
27:
28: io_process: process
29:    variable out_line: line;
30:
31: begin
32:
33: s01 <= '1';
34: s11 <= '1';
35: en1 <= '0';
36:
37: wait for 10 ns;
38:
39: s01 <= '0';
40: s11 <= '0';
41: en1 <= '1';
42:
43: wait for 10 ns;
44:
45: s01 <= '0';
46: s11 <= '1';
47: en1 <= '1';
48:
49: wait for 10 ns;
50:
51: s01 <= '1';
52: s11 <= '0';
53: en1 <= '1';
54:
55: wait for 10 ns;
56:
57: s01 <= '1';
58: s11 <= '1';
59: en1 <= '1';
60:
61: wait for 10 ns;
62:
63: print_output;
64:
65: end process;
66:
67: end test;
68:
```

```
    1: library IEEE;
    2: use IEEE.STD_LOGIC_1164.ALL;
    3:
    4:
    5: entity decoder_3to8 is
    6: port(input1,input2, input3: in std_logic;
    7: output: out std_logic_vector(7 downto 0));
    8: end decoder_3to8;
    9:
   10: architecture structural of decoder_3to8 is
   11:
   12: component decoder_2to4
   13: port(input1,input2,en : in std_logic;
   14: output : out std_logic_vector(3 downto 0));
   15: end component;
   16:
   17: component inverter
   18:  port (
   19:    input    : in  std_logic;
   20:    output   : out std_logic);
   21: end component;
   22:
   23: for decoder_2to4_1,decoder_2to4_2 : decoder_2to4 use entity work.decoder_2to4(
structural);
   24: for inv_1 : inverter use entity work.inverter(structural);
   25:
   26: signal input3_b :std_logic;
   27:
   28: begin
   29: inv_1 :inverter port map(input3, input3_b);
   30: decoder_2to4_1 : decoder_2to4 port map(input1,input2,input3_b,output(3 downto
0));
   31: decoder_2to4_2 : decoder_2to4 port map(input1,input2,input3,output(7 downto 4)
);
   32:
   33: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity dff is
 6:   port ( d   : in  std_logic;
 7:          clk : in  std_logic;
 8:          q   : out std_logic);
 9: end dff;
10:
11: architecture structural of dff is
12: begin
13:
14:   output: process
15:
16:   begin
17:     wait until ( clk'EVENT and clk = '0' );
18:     q <= d;
19:   end process output;
20:
21:
22: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity Dlatch is
 6:   port ( d   : in  std_logic;
 7:          clk : in  std_logic;
 8:          q   : out std_logic);
 9: end Dlatch;
10:
11: architecture structural of Dlatch is
12:
13: begin
14:
15:   output: process (d,clk)
16:
17:   begin
18:     if clk = '1' then
19:     q <= d;
20:  end if;
21:  end process output;
22:
23: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity hit_miss is
 6:   port (
 7:     tag_valid_data   : in  std_logic_vector(3 downto 0);
 8:     CA_data   : in  std_logic_vector(2 downto 0);
 9:     reset: in  std_logic;
10:     hm_signal : out std_logic);
11: end hit_miss;
12:
13: architecture structural of hit_miss is
14:
15: component xor2
16:   port (
17:     input1   : in  std_logic;
18:     input2   : in  std_logic;
19:     output   : out std_logic);
20: end component;
21:
22: component and2
23:   port (
24:     input1   : in  std_logic;
25:     input2   : in  std_logic;
26:     output   : out std_logic);
27: end component;
28:
29: component nor3
30:   port(input1 :in std_logic;
31:      input2 : in std_logic;
32:      input3 : in std_logic;
33:      output : out std_logic);
34: end component;
35:
36: component inverter
37:   port(input :in std_logic;
38:      output : out std_logic);
39: end component;
40:
41: for all: xor2 use entity work.xor2(structural);
42: for all : and2 use entity work.and2(structural);
43: for all : nor3 use entity work.nor3(structural);
44: for all : inverter use entity work.inverter(structural);
45:
46:
47: signal temp : std_logic_vector(3 downto 0);
48: signal reset_b,temp1: std_logic;
49: begin
50: inv_1 :inverter port map (reset,reset_b);
51: xor2_1 : xor2 port map (CA_data(0),tag_valid_data(0),temp(0));
52: xor2_2 : xor2 port map (CA_data(1),tag_valid_data(1),temp(1));
53: xor2_3 : xor2 port map (CA_data(2),tag_valid_data(2),temp(2));
54: nor3_1  : nor3 port map (temp(0),temp(1),temp(2),temp(3));
55: and2_1 : and2 port map (temp(3), tag_valid_data(3), temp1);
56: and2_2: and2 port map (temp1, reset_b, hm_signal);
57: end structural;
58:
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity inverter is
 6:   port (
 7:     input    : in  std_logic;
 8:     output   : out std_logic);
 9: end inverter;
10:
11: architecture structural of inverter is
12:
13: begin
14:
15:   output <= not (input);
16:
17: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity LRU_cell is
 6: port ( reset, read_m_en :  in std_logic;
 7:        LRU_signal : out std_logic);
 8: end LRU_cell;
 9:
10: architecture structural of LRU_cell is
11:
12: component dff
13: port (   d   : in  std_logic;
14:          clk : in  std_logic;
15:          q   : out std_logic);
16: end component;
17:
18: component or2
19: port (   input1 : in std_logic;
20:          input2 : in std_logic;
21:          output:out std_logic);
22: end component;
23:
24: component and2
25: port(input1 : in std_logic;
26:      input2 : in std_logic;
27:      output : out std_logic);
28: end component;
29:
30: component inverter
31: port (
32:     input    : in  std_logic;
33:     output   : out std_logic);
34: end component;
35:
36: component buff
37: port (
38:     input    : in  std_logic;
39:     output   : out std_logic);
40: end component;
41:
42:
43: for all : dff use entity work.dff(structural);
44: for all : or2 use entity work.or2(structural);
45: for all : inverter use entity work.inverter(structural);
46: for all : and2 use entity work.and2(structural);
47: for all : buff use entity work.buff(structural);
48:
49:
50: signal reset_b, q_b, clk_b,clk, q, d: std_logic;
51:
52: begin
53:
54: or2_1 : or2 port map (reset, read_m_en,clk_b);
55: inv_3 : inverter port map(clk_b,clk);
56: inv_1 : inverter port map(reset,reset_b);
57: inv_2 : inverter port map(q,q_b);
58: and2_1 : and2 port map (q_b, reset_b,d);
59: dff_1: dff port map(d,clk,q);
60: buff_1: buff port map(q,LRU_signal);
61: end structural;
```

```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity mux_2to1_bit is
    6:
    7:   port (
    8:     A  : in  std_logic;
    9:     B  : in  std_logic;
   10:     sel: in  std_logic;
   11:     output   : out std_logic
   12: );
   13: end mux_2to1_bit;
   14:
   15: architecture structural of mux_2to1_bit is
   16:
   17:         component tristate_buffer
   18:         port ( input    : in  STD_LOGIC;
   19:                    en   : in  STD_LOGIC;
   20:                output   : out STD_LOGIC);
   21:         end component;
   22:
   23:         component inverter
   24:         port( input : in std_logic;
   25:               output : out std_logic);
   26:         end component;
   27:
   28: for inv_1 : inverter use entity work.inverter(structural);
   29: for tristate_buffer_0,tristate_buffer_1 : tristate_buffer use entity work.tris
tate_buffer(structural);
   30: signal sel_b: std_logic;
   31:
   32: begin
   33:
   34:  inv_1 : inverter port map(sel,sel_b);
   35:  tristate_buffer_0 : tristate_buffer port map(A,sel_b,output);
   36:  tristate_buffer_1 : tristate_buffer port map(B,sel,output);
   37:
   38: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity mux_2to1_byte is
 6:   port (
 7:     A  : in  std_logic_vector(7 downto 0);
 8:     B  : in  std_logic_vector(7 downto 0);
 9:     sel: in  std_logic;
10:     output   : out std_logic_vector(7 downto 0));
11: end mux_2to1_byte;
12:
13: architecture structural of mux_2to1_byte is
14:
15: component mux_2to1_bit
16:  port( A  : in  std_logic;
17:        B  : in  std_logic;
18:        sel: in  std_logic;
19:        output   : out std_logic);
20: end component;
21:
22:
23: for all : mux_2to1_bit use entity work.mux_2to1_bit(structural);
24:
25:
26: begin
27:
28: mux_2to1_bit_0 : mux_2to1_bit port map (A(0),B(0),sel,output(0));
29: mux_2to1_bit_1 : mux_2to1_bit port map (A(1),B(1),sel,output(1));
30: mux_2to1_bit_2 : mux_2to1_bit port map (A(2),B(2),sel,output(2));
31: mux_2to1_bit_3 : mux_2to1_bit port map (A(3),B(3),sel,output(3));
32: mux_2to1_bit_4 : mux_2to1_bit port map (A(4),B(4),sel,output(4));
33: mux_2to1_bit_5 : mux_2to1_bit port map (A(5),B(5),sel,output(5));
34: mux_2to1_bit_6 : mux_2to1_bit port map (A(6),B(6),sel,output(6));
35: mux_2to1_bit_7 : mux_2to1_bit port map (A(7),B(7),sel,output(7));
36:
37: end structural;
```

```
 1: library IEEE;
 2: use IEEE.STD_LOGIC_1164.ALL;
 3:
 4:
 5: entity nor2 is
 6: port(input1 :in std_logic;
 7:      input2 : in std_logic;
 8:      output : out std_logic);
 9: end nor2;
10:
11: architecture structural of nor2 is
12:
13: begin
14:
15: output <= input1 nor input2;
16:
17: end structural;
```

```
 1: library IEEE;
 2: use IEEE.STD_LOGIC_1164.ALL;
 3:
 4:
 5: entity nor3 is
 6: port(input1 :in std_logic;
 7:      input2 : in std_logic;
 8:      input3 : in std_logic;
 9:      output : out std_logic);
10: end nor3;
11:
12: architecture structural of nor3 is
13:
14: component nor2
15: port(input1 : in std_logic;
16: input2 : in std_logic;
17: output : out std_logic);
18: end component;
19:
20: for nor2_1, nor2_2 : nor2 use entity work.nor2(structural);
21: signal temp: std_logic;
22: begin
23:
24: nor2_1 : nor2 port map(input1, input2, temp);
25: nor2_2 : nor2 port map(input3, temp, output);
26:
27: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity or2 is
 6:
 7: port (
 8:     input1    : in  std_logic;
 9:     input2 : in std_logic;
10:     output   : out std_logic);
11: end or2;
12:
13: architecture structural of or2 is
14:
15: begin
16:
17:   output <= input1  or input2;
18:
19: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity or3 is
 6: port(input1 : in std_logic;
 7:      input2 : in std_logic;
 8:      input3 : in std_logic;
 9:      output : out std_logic);
10: end or3;
11:
12: architecture structural of or3 is
13:
14: component or2
15: port(input1 : in std_logic;
16: input2 : in std_logic;
17: output : out std_logic);
18: end component;
19:
20: for all : or2 use entity work.or2(structural);
21:
22: signal temp: std_logic;
23:
24: begin
25: or2_1 : or2 port map(input1, input2, temp);
26: or2_2 : or2 port map(input3, temp, output);
27: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity or8 is
 6: port(input1 : in std_logic_vector (7 downto 0);
 7:      input2 : in std_logic_vector (7 downto 0);
 8:      output : out std_logic_vector (7 downto 0));
 9: end or8;
10:
11: architecture structural of or8 is
12:
13: component or2
14: port(input1 : in std_logic;
15: input2 : in std_logic;
16: output : out std_logic);
17: end component;
18:
19: for all : or2 use entity work.or2(structural);
20:
21:
22: begin
23: or2_1 : or2 port map(input1(0), input2(0), output(0));
24: or2_2 : or2 port map(input1(1), input2(1), output(1));
25: or2_3 : or2 port map(input1(2), input2(2), output(2));
26: or2_4 : or2 port map(input1(3), input2(3), output(3));
27: or2_5 : or2 port map(input1(4), input2(4), output(4));
28: or2_6 : or2 port map(input1(5), input2(5), output(5));
29: or2_7 : or2 port map(input1(6), input2(6), output(6));
30: or2_8 : or2 port map(input1(7), input2(7), output(7));
31: end structural;
```

```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity register_8bit is
    6:   port ( d   : in  std_logic_vector(7 downto 0);
    7:          clk : in  std_logic;
    8:          q   : out std_logic_vector(7 downto 0));
    9: end register_8bit;
   10:
   11: architecture structural of register_8bit is
   12:
   13: component dff
   14:   port ( d   : in  std_logic;
   15:          clk : in  std_logic;
   16:          q   : out std_logic);
   17: end component;
   18:
   19: for dff_0, dff_1, dff_2, dff_3, dff_4, dff_5, dff_6, dff_7 : dff use entity wo
rk.dff(structural);
   20:
   21: begin
   22:
   23: dff_0 : dff port map(d(0),clk,q(0));
   24: dff_1 : dff port map(d(1),clk,q(1));
   25: dff_2 : dff port map(d(2),clk,q(2));
   26: dff_3 : dff port map(d(3),clk,q(3));
   27: dff_4 : dff port map(d(4),clk,q(4));
   28: dff_5 : dff port map(d(5),clk,q(5));
   29: dff_6 : dff port map(d(6),clk,q(6));
   30: dff_7 : dff port map(d(7),clk,q(7));
   31:
   32:
   33: end structural;
```

```
 1: library IEEE;
 2: use IEEE.STD_LOGIC_1164.ALL;
 3:
 4:
 5: entity r_m_control is
 6: port(input: in std_logic_vector(7 downto 0);
 7:      s0,s1,w_cache : out std_logic
 8:      );
 9: end r_m_control;
10:
11: architecture structural of r_m_control is
12:
13: component or2
14: port(
15:     input1    : in  std_logic;
16:     input2 : in std_logic;
17:     output   : out std_logic);
18: end component;
19:
20: component buff
21: port(
22: input : in std_logic;
23: output : out std_logic);
24: end component;
25:
26: for all : buff use entity work.buff(structural);
27: for all : or2 use entity work.or2(structural);
28:
29: signal temp : std_logic_vector(5 downto 0);
30:
31: begin
32:
33: or2_1 : or2 port map(input(0),input(1),temp(0));
34: or2_2 : or2 port map(input(2),input(3),temp(1));
35: or2_3 : or2 port map(input(4),input(5),temp(2));
36: or2_4 : or2 port map(input(6),input(7),temp(3));
37: or2_5 : or2 port map(temp(0),temp(1),temp(4));
38: or2_6 : or2 port map(temp(2),temp(3),temp(5));
39: or2_7 : or2 port map(temp(4),temp(5),w_cache);
40: or2_8 : or2 port map(temp(1),temp(3),s0);
41: buff_1: buff port map(temp(5),s1);
42: end structural;
```

```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity state_machine is
    6: port(clk, reset, start, read_m,read_h,write_m,write_h : in std_logic;
    7: state0_en,state0_loop,read_h_en,write_h_en,read_m_en,memory_en,read_en,op_busy
 : out std_logic;
    8: data_receive: out std_logic_vector(7 downto 0));
    9: end state_machine;
   10:
   11: architecture structural of state_machine is
   12:
   13: component dff
   14:   port ( d   : in  std_logic;
   15:          clk : in  std_logic;
   16:          q   : out std_logic);
   17: end component;
   18:
   19: component and2
   20: port(input1 : in std_logic;
   21:      input2 : in std_logic;
   22:      output : out std_logic);
   23: end component;
   24:
   25: component or2
   26: port(
   27:     input1    : in  std_logic;
   28:     input2 : in std_logic;
   29:     output   : out std_logic);
   30: end component;
   31:
   32: component inverter
   33:  port (
   34:     input    : in  std_logic;
   35:     output   : out std_logic);
   36: end component;
   37:
   38: component buff
   39:  port (
   40:    input : in std_logic;
   41:    output : out std_logic);
   42: end component;
   43:
   44: for all : dff use entity work.dff(structural);
   45: for all : and2 use entity work.and2(structural);
   46: for all : or2 use entity work.or2(structural);
   47: for all : inverter use entity work.inverter(structural);
   48: for all : buff use entity work.buff(structural);
   49:
   50:
   51: signal start_b,reset_b:std_logic;
   52: -----state 0 signal----
   53: signal state_0_loop,state_0_en       :std_logic;
   54: signal temp :std_logic_vector(6 downto 0);
   55: -----hit/miss---signal----
   56: signal read_h_state  :std_logic_vector(1 downto 0);
   57: signal write_h_state :std_logic_vector(3 downto 0);
   58: signal read_m_state,temp1  :std_logic_vector (17 downto 0);
   59: signal write_m_state :std_logic_vector (3 downto 0);
   60:
   61: begin
   62: inv_1 : inverter port map(start,start_b);
   63: inv_2 : inverter port map(reset, reset_b);
   64:
   65: ---------------state 0-----------------------
   66: and2_1 : and2 port map(state_0_loop,start_b,temp(0));
   67: or2_1 : or2 port map(temp1(17),read_h_state(1),temp(1));
   68: or2_2 : or2 port map(write_m_state(3),write_h_state(3),temp(2));
   69: or2_3 : or2 port map(temp(1),temp(2),temp(3));
   70: or2_4 : or2 port map(temp(3), reset, temp(4));
   71: or2_5 : or2 port map(temp(0),temp(4),temp(5));
   72: dff_1 : dff port map(temp(5),clk,state_0_loop);
   73: and2_2 : and2 port map(state_0_loop,start, temp(6));
   74: dff_2 : dff port map(temp(6), clk, state_0_en);
   75: buff_1: buff port map(temp(3),op_busy);
   76: buff_2: buff port map(state_0_loop,state0_loop);
   77: buff_3: buff port map(state_0_en,state0_en);
   78: ---------------Read Hit--------------------
   79: and2_3 : and2 port map(state_0_en,read_h,read_h_state(0));
   80: dff_3 : dff port map(read_h_state(0),clk,read_h_state(1));
   81: buff_4: buff port map(read_h_state(1),read_h_en);
   82: ---------------Write Hit--------------------
   83: and2_4 : and2 port map(state_0_en,write_h,write_h_state(0));
   84: dff_4 : dff port map(write_h_state(0), clk,write_h_state(1));
   85: and2_5 : and2 port map(write_h_state(1),reset_b,write_h_state(2));
   86: dff_5 : dff port map(write_h_state(2), clk,write_h_state(3));
   87: buff_5: buff port map(write_h_state(1),write_h_en);
   88: ---------------Read Miss--------------------
   89: and2_6 :and2 port map(state_0_en,read_m,read_m_state(0));
   90: dff_6 : dff port map(read_m_state(0),clk,temp1(0));
   91: buff_6: buff port map(temp1(0),memory_en);
   92: and2_7 :and2 port map(temp1(0),reset_b,read_m_state(1));
   93: dff_7  : dff port map(read_m_state(1),clk,temp1(1));
   94: and2_8 : and2 port map(temp1(1),reset_b,read_m_state(2));
   95: dff_8 : dff port map(read_m_state(2),clk,temp1(2));
   96: and2_9 : and2 port map(temp1(2), reset_b,read_m_state(3));
   97: dff_9 : dff port map(read_m_state(3),clk,temp1(3));
   98: and2_10 : and2 port map(temp1(3), reset_b, read_m_state(4));
   99: dff_10 : dff port map(read_m_state(4),clk,temp1(4));
  100: and2_11 : and2 port map(temp1(4), reset_b,read_m_state(5));
  101: dff_11 : dff port map(read_m_state(5),clk,temp1(5));
  102: and2_12 : and2 port map(temp1(5), reset_b,read_m_state(6));
  103: dff_12 : dff port map(read_m_state(6),clk,temp1(6));
  104: and2_13 : and2 port map(temp1(6), reset_b,read_m_state(7));
  105: dff_13 : dff port map(read_m_state(7),clk,temp1(7));
  106: buff_7: buff port map(temp1(7),data_receive(0));
  107: and2_14 : and2 port map(temp1(7), reset_b,read_m_state(8));
  108: dff_14 : dff port map(read_m_state(8),clk,temp1(8));
  109: buff_8: buff port map(temp1(8),data_receive(1));
  110: and2_15 : and2 port map(temp1(8), reset_b,read_m_state(9));
  111: dff_15 : dff port map(read_m_state(9),clk,temp1(9));
  112: buff_9: buff port map(temp1(9),data_receive(2));
  113: and2_16 : and2 port map(temp1(9), reset_b,read_m_state(10));
  114: dff_16 : dff port map(read_m_state(10),clk,temp1(10));
  115: buff_10: buff port map(temp1(10),data_receive(3));
  116: and2_17 : and2 port map(temp1(10), reset_b,read_m_state(11));
  117: dff_17 : dff port map(read_m_state(11),clk,temp1(11));
  118: buff_11: buff port map(temp1(11),data_receive(4));
  119: and2_18: and2 port map(temp1(11), reset_b,read_m_state(12));
  120: dff_18 : dff port map(read_m_state(12),clk,temp1(12));
  121: buff_12: buff port map(temp1(12),data_receive(5));
  122: and2_19 : and2 port map(temp1(12), reset_b,read_m_state(13));
  123: dff_19 : dff port map(read_m_state(13),clk,temp1(13));
```

```
124: buff_13: buff port map(temp1(13),data_receive(6));
125: and2_20 : and2 port map(temp1(13), reset_b,read_m_state(14));
126: dff_20 : dff port map(read_m_state(14),clk,temp1(14));
127: buff_14: buff port map(temp1(14),data_receive(7));
128: and2_21 : and2 port map(temp1(14), reset_b,read_m_state(15));
129: dff_21 : dff port map(read_m_state(15),clk,temp1(15));
130: buff_15: buff port map(temp1(15),read_en);
131: and2_22 : and2 port map(temp1(15), reset_b,read_m_state(16));
132: dff_22 : dff port map(read_m_state(16),clk,temp1(16));
133: and2_23 : and2 port map(temp1(16), reset_b,read_m_state(17));
134: dff_23 : dff port map(read_m_state(17),clk,temp1(17));
135: buff_16: buff port map(temp1(17),read_m_en);
136: ---------------Write Miss--------------------
137: and2_24 : and2 port map(state_0_en,write_m,write_m_state(0));
138: dff_24 : dff port map(write_m_state(0), clk,write_m_state(1));
139: and2_25 : and2 port map(write_m_state(1),reset_b,write_m_state(2));
140: dff_25 : dff port map(write_m_state(2),clk,write_m_state(3));
141: end structural;
```

```
    1:
    2: library STD;
    3: library IEEE;
    4: use IEEE.std_logic_1164.all;
    5: use IEEE.std_logic_textio.all;
    6: use STD.textio.all;
    7:
    8: entity state_machine_test is
    9:
   10: end state_machine_test;
   11:
   12: architecture test of state_machine_test is
   13:
   14: component state_machine
   15: port ( clk, reset, start, read_m,read_h,write_m,write_h : in std_logic;
   16: state0_en,state0_loop,read_h_en,write_h_en,read_m_en,memory_en,read_en,op_busy
 : out std_logic;
   17: data_receive: out std_logic_vector(7 downto 0));
   18: end component;
   19:
   20: for state_machine_1: state_machine use entity work.state_machine(structural);
   21: signal clk1,reset1,start1,r_m1,r_h1,w_m1,w_h1,clock: std_logic;
   22:
   23: procedure print_output is
   24:    variable out_line: line;
   25:
   26:    begin
   27: --   write (out_line, string'(" din1:"));
   28: --   write (out_line, din1);
   29: ----   write (out_line, string'(" en1:"));
   30: ----   write (out_line, en1);
   31: --   write (out_line, string'(" rw_en1:"));
   32: --   write (out_line, rw_en1);
   33: --   writeline(output, out_line);
   34: --   write (out_line, string'(" dout:"));
   35: --   write (out_line, dout1);
   36: --   writeline(output, out_line);
   37: end print_output;
   38:
   39: begin
   40:
   41:   clk1 <= clock;
   42: state_machine_1 : state_machine port map (clk1,reset1,start1,r_m1,r_h1,w_m1,w_
h1);
   43:
   44:   clking : process
   45:   begin
   46:     clock<= '1', '0' after 5 ns;
   47:     wait for 10 ns;
   48:   end process clking;
   49:
   50: io_process: process
   51:    variable out_line: line;
   52:
   53: begin
   54:
   55: reset1 <= '1';
   56: start1 <= '0';
   57: r_m1 <= '0';
   58: r_h1 <= '0';
   59: w_m1 <= '0';
   60: w_h1 <= '0';
   61: wait for 20 ns;
   62:
   63: reset1 <= '1';
   64:
   65: wait for 10 ns;
   66:
   67: reset1 <= '0';
   68:
   69: wait for 15 ns;
   70:
   71: start1 <= '1';
   72: w_m1 <= '1';
   73: wait for 10 ns;
   74:
   75: start1 <= '1';
   76: wait for 10 ns;
   77: start1 <= '1';
   78: w_m1 <= '1';
   79: wait for 10 ns;
   80: start1 <= '0';
   81: w_m1<='0';
   82: wait for 200 ns;
   83: reset1 <= '1';
   84: wait for 10 ns;
   85: reset1 <= '0';
   86:
   87: wait for 50 ns;
   88:
   89: print_output;
   90:
   91: end process;
   92:
   93: end test;
```

```
    1: library IEEE;
    2: use IEEE.STD_LOGIC_1164.ALL;
    3:
    4:
    5: entity tag_valid_block is
    6: Port ( block_en : in std_logic_vector(7 downto 0);
    7:        reset,cache_tag_rw : in std_logic;
    8:        CA_reg : in std_logic_vector(2 downto 0);
    9:        tag_valid_data : out std_logic_vector(3 downto 0));
   10: end tag_valid_block;
   11:
   12: architecture structural of tag_valid_block is
   13:
   14: component inverter
   15:  port (
   16:     input    : in  std_logic;
   17:     output   : out std_logic);
   18: end component;
   19:
   20: component or2
   21: port(
   22:     input1    : in  std_logic;
   23:     input2 : in std_logic;
   24:     output   : out std_logic);
   25: end component;
   26:
   27: component nor2
   28: port(input1 : in std_logic;
   29:      input2 : in std_logic;
   30:      output : out std_logic);
   31: end component;
   32:
   33: component xnor2
   34: port(input1 : in std_logic;
   35:      input2 : in std_logic;
   36:      output : out std_logic);
   37: end component;
   38:
   39:
   40: component tag_valid_block_cell
   41: port ( w_data :  in std_logic_vector(3 downto 0);
   42:        byte_en : in std_logic;
   43:        rw_en : in std_logic;
   44:        r_data : out std_logic_vector(3 downto 0));
   45: end component;
   46:
   47: for all : inverter use entity work.inverter(structural);
   48: for all : or2 use entity work.or2(structural);
   49: for all : nor2 use entity work.nor2(structural);
   50: for all : xnor2 use entity work.nor2(structural);
   51: for all : tag_valid_block_cell use entity work.tag_valid_block_cell(structural
);
   52:
   53: signal block_temp_en : std_logic_vector(7 downto 0);
   54: signal temp          : std_logic_vector(2 downto 0);
   55: signal tag_valid_data1: std_logic_vector(3 downto 0);
   56: signal rw_en         : std_logic;
   57:
   58: begin
   59: or2_0 : or2 port map(block_en(0),reset,block_temp_en(0));
   60: or2_1 : or2 port map(block_en(1),reset,block_temp_en(1));
   61: or2_2 : or2 port map(block_en(2),reset,block_temp_en(2));
   62: or2_3 : or2 port map(block_en(3),reset,block_temp_en(3));
   63: or2_4 : or2 port map(block_en(4),reset,block_temp_en(4));
   64: or2_5 : or2 port map(block_en(5),reset,block_temp_en(5));
   65: or2_6 : or2 port map(block_en(6),reset,block_temp_en(6));
   66: or2_7 : or2 port map(block_en(7),reset,block_temp_en(7));
   67:
   68:
   69: inv_1 : inverter port map(CA_reg(2), temp(2));
   70: inv_2 : inverter port map(CA_reg(1), temp(1));
   71: inv_3 : inverter port map(CA_reg(0), temp(0));
   72: inv_4 : inverter port map(reset, tag_valid_data1(3));
   73:
   74: nor2_1 : nor2 port map(temp(2),reset,tag_valid_data1(2));
   75: nor2_2 : nor2 port map(temp(1),reset,tag_valid_data1(1));
   76: nor2_3 : nor2 port map(temp(0),reset,tag_valid_data1(0));
   77: xnor2_3: xnor2 port map(cache_tag_rw,reset,rw_en);
   78:
   79:
   80: tag_valid_block_cell_0 : tag_valid_block_cell port map(tag_valid_data1, block_
temp_en(0),rw_en,tag_valid_data);
   81: tag_valid_block_cell_1 : tag_valid_block_cell port map(tag_valid_data1, block_
temp_en(1),rw_en,tag_valid_data);
   82: tag_valid_block_cell_2 : tag_valid_block_cell port map(tag_valid_data1, block_
temp_en(2),rw_en,tag_valid_data);
   83: tag_valid_block_cell_3 : tag_valid_block_cell port map(tag_valid_data1, block_
temp_en(3),rw_en,tag_valid_data);
   84: tag_valid_block_cell_4 : tag_valid_block_cell port map(tag_valid_data1, block_
temp_en(4),rw_en,tag_valid_data);
   85: tag_valid_block_cell_5 : tag_valid_block_cell port map(tag_valid_data1, block_
temp_en(5),rw_en,tag_valid_data);
   86: tag_valid_block_cell_6 : tag_valid_block_cell port map(tag_valid_data1, block_
temp_en(6),rw_en,tag_valid_data);
   87: tag_valid_block_cell_7 : tag_valid_block_cell port map(tag_valid_data1, block_
temp_en(7),rw_en,tag_valid_data);
   88:
   89:
   90:
   91: end structural;
```

```
    1: library STD;
    2: library IEEE;
    3: use IEEE.std_logic_1164.all;
    4:
    5: entity tag_valid_block_cell is
    6: port ( w_data :  in std_logic_vector(3 downto 0);
    7:        byte_en : in std_logic;
    8:        rw_en : in std_logic;
    9:        r_data : out std_logic_vector(3 downto 0));
   10: end tag_valid_block_cell;
   11:
   12: architecture structural of tag_valid_block_cell is
   13:
   14: component cache_bit_cell
   15: port ( w_data :  in std_logic;
   16:        bit_en : in std_logic;
   17:        rw_en : in std_logic;
   18:        r_data : out std_logic);
   19: end component;
   20:
   21: for cache_bit_cell_0, cache_bit_cell_1,cache_bit_cell_2,cache_bit_cell_3: cach
e_bit_cell use entity work.cache_bit_cell(structural);
   22:
   23: begin
   24: cache_bit_cell_0 : cache_bit_cell port map(w_data(0),byte_en,rw_en,r_data(0));
   25: cache_bit_cell_1 : cache_bit_cell port map(w_data(1),byte_en,rw_en,r_data(1));
   26: cache_bit_cell_2 : cache_bit_cell port map(w_data(2),byte_en,rw_en,r_data(2));
   27: cache_bit_cell_3 : cache_bit_cell port map(w_data(3),byte_en,rw_en,r_data(3));
   28: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.STD_LOGIC_1164.ALL;
 4: entity tristate_buffer is
 5:
 6:   Port ( input    : in  STD_LOGIC;
 7:          en    : in  STD_LOGIC;
 8:          output    : out STD_LOGIC);
 9: end tristate_buffer;
10:
11: architecture structural of tristate_buffer is
12:
13: component tx
14:   port ( sel    : in std_logic;
15:        selnot: in std_logic;
16:        input : in std_logic;
17:        output:out std_logic);
18: end component;
19:
20: component inverter
21: port (input : in std_logic;
22: output : out std_logic);
23: end component;
24:
25: for tx_1 : tx use entity work.tx(structural);
26: for inv_1 : inverter use entity work.inverter(structural);
27:
28: signal en_b:std_logic;
29: begin
30:
31: inv_1 : inverter port map (en, en_b);
32: tx_1 : tx port map (en, en_b,input,output);
33: end structural;
```

```
    1: library STD;
    2: library IEEE;
    3: use IEEE.STD_LOGIC_1164.ALL;
    4: entity tristate_buffer_8bit is
    5:
    6:   Port ( input    : in  STD_LOGIC_VECTOR(7 downto 0);
    7:          en   : in  STD_LOGIC;
    8:          output    : out STD_LOGIC_VECTOR(7 downto 0));
    9: end tristate_buffer_8bit;
   10:
   11: architecture structural of tristate_buffer_8bit is
   12:
   13: component tristate_buffer
   14:   Port ( input    : in  STD_LOGIC;
   15:          en   : in  STD_LOGIC;
   16:          output    : out STD_LOGIC);
   17: end component;
   18:
   19: for tristate_buffer_0, tristate_buffer_1,tristate_buffer_2,tristate_buffer_3,t
ristate_buffer_4, tristate_buffer_5,tristate_buffer_6,tristate_buffer_7 : tristate_buf
fer use entity work.tristate_buffer(structural);
   20:
   21: begin
   22: tristate_buffer_0 : tristate_buffer port map(input(0),en,output(0));
   23: tristate_buffer_1 : tristate_buffer port map(input(1),en,output(1));
   24: tristate_buffer_2 : tristate_buffer port map(input(2),en,output(2));
   25: tristate_buffer_3 : tristate_buffer port map(input(3),en,output(3));
   26: tristate_buffer_4 : tristate_buffer port map(input(4),en,output(4));
   27: tristate_buffer_5 : tristate_buffer port map(input(5),en,output(5));
   28: tristate_buffer_6 : tristate_buffer port map(input(6),en,output(6));
   29: tristate_buffer_7 : tristate_buffer port map(input(7),en,output(7));
   30: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity tx is
 6:   port ( sel   : in std_logic;
 7:          selnot: in std_logic;
 8:          input : in std_logic;
 9:          output:out std_logic);
10: end tx;
11:
12: architecture structural of tx is
13:
14: begin
15:
16:   txprocess: process (sel, selnot, input)
17:   begin
18:     if (sel = '1' and selnot = '0') then
19:       output <= input;
20:     else
21:       output <= 'Z';
22:     end if;
23:   end process txprocess;
24:
25: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity xnor2 is
 6:   port(
 7:   input1 : in std_logic;
 8:   input2 : in std_logic;
 9:   output : out std_logic);
10: end xnor2;
11:
12: architecture structural of xnor2 is
13:
14: component inverter
15: port(input : in std_logic;
16:      output : out std_logic);
17: end component;
18:
19: component xor2
20: port(
21:   input1 : in std_logic;
22:   input2 : in std_logic;
23:   output : out std_logic);
24: end component;
25:
26:
27: for inv_1 : inverter use entity work.inverter(structural);
28: for xor2_1 : xor2 use entity work.xor2(structural);
29:
30: signal temp:std_logic;
31:
32: begin
33:
34: xor2_1 : xor2 port map(input1, input2, temp);
35: inv_1 : inverter port map(temp, output);
36:
37:
38: end structural;
```

```
 1: library STD;
 2: library IEEE;
 3: use IEEE.std_logic_1164.all;
 4:
 5: entity xor2 is
 6:
 7:   port (
 8:     input1   : in  std_logic;
 9:     input2   : in  std_logic;
10:     output   : out std_logic);
11: end xor2;
12:
13: architecture structural of xor2 is
14:
15: begin
16:
17:   output <= input2 xor input1;
18:
19: end structural;
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          58              nets
   12:          13              terminals
   13:          53              pmos
   14:          53              nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          58              nets
   19:          13              terminals
   20:          53              pmos
   21:          53              nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N45       N0        gnd!
   26:     N49       N9        input1
   27:     N48       N8        input2
   28:     N46       N2        input3
   29:     N57       N13       output<0>
   30:     N56       N12       output<1>
   31:     N55       N11       output<2>
   32:     N54       N10       output<3>
   33:     N53       N6        output<4>
   34:     N51       N5        output<5>
   35:     N50       N4        output<6>
   36:     N47       N3        output<7>
   37:     N52       N1        vdd!
   38:
   39: Devices in the netlist but not in the rules:
   40:          pcapacitor
   41: Devices in the rules but not in the netlist:
   42:          cap nfet pfet nmos4 pmos4
   43:
   44: The net-lists match.
   45:
   46:                                 layout  schematic
   47:                                    instances
   48:          un-matched                0       0
   49:          rewired                   0       0
   50:          size errors               0       0
   51:          pruned                    0       0
   52:          active                  106     106
   53:          total                   106     106
   54:
   55:                                      nets
   56:          un-matched                0       0
   57:          merged                    0       0
   58:          pruned                    0       0
   59:          active                   58      58
   60:          total                    58      58
   61:
   62:                                    terminals
   63:          un-matched                0       0
   64:          matched but
   65:          different type            0       0
   66:          total                    13      13
   67:
   68:
   69: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   70:
   71: devbad.out:
   72:
   73: netbad.out:
   74:
   75: mergenet.out:
   76:
   77: termbad.out:
   78:
   79: prunenet.out:
   80:
   81: prunedev.out:
   82:
   83: audit.out:
   84:
   85:
   86: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   87:
   88: devbad.out:
   89:
   90: netbad.out:
   91:
   92: mergenet.out:
   93:
   94: termbad.out:
   95:
   96: prunenet.out:
   97:
   98: prunedev.out:
   99:
  100: audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          7               nets
   12:          5               terminals
   13:          3               pmos
   14:          3               nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          7               nets
   19:          5               terminals
   20:          3               pmos
   21:          3               nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N2          N1          gnd!
   26:     N4          N3          input1
   27:     N3          N2          input2
   28:     N5          N4          output
   29:     N6          N0          vdd!
   30:
   31: Devices in the netlist but not in the rules:
   32:          pcapacitor
   33: Devices in the rules but not in the netlist:
   34:          cap nfet pfet nmos4 pmos4
   35:
   36: The net-lists match.
   37:
   38:                                 layout  schematic
   39:                                   instances
   40:          un-matched               0       0
   41:          rewired                  0       0
   42:          size errors              0       0
   43:          pruned                   0       0
   44:          active                   6       6
   45:          total                    6       6
   46:
   47:                                     nets
   48:          un-matched               0       0
   49:          merged                   0       0
   50:          pruned                   0       0
   51:          active                   7       7
   52:          total                    7       7
   53:
   54:                                   terminals
   55:          un-matched               0       0
   56:          matched but
   57:          different type           0       0
   58:          total                    5       5
   59:
   60:
   61: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   62:
   63: devbad.out:
   64:
   65: netbad.out:
   66:
   67: mergenet.out:
   68:
   69: termbad.out:
   70:
   71: prunenet.out:
   72:
   73: prunedev.out:
   74:
   75: audit.out:
   76:
   77:
   78: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   79:
   80: devbad.out:
   81:
   82: netbad.out:
   83:
   84: mergenet.out:
   85:
   86: termbad.out:
   87:
   88: prunenet.out:
   89:
   90: prunedev.out:
   91:
   92: audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
          7               nets
          5               terminals
          3               pmos
          3               nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
          7               nets
          5               terminals
          3               pmos
          3               nmos


    Terminal correspondence points
    N2        N1        gnd!
    N4        N3        input1
    N3        N2        input2
    N5        N4        output
    N6        N0        vdd!

Devices in the netlist but not in the rules:
         pcapacitor
Devices in the rules but not in the netlist:
         cap nfet pfet nmos4 pmos4

The net-lists match.

                                layout  schematic
                                  instances
         un-matched               0       0
         rewired                  0       0
         size errors              0       0
         pruned                   0       0
         active                   6       6
         total                    6       6

                                    nets
         un-matched               0       0
         merged                   0       0
         pruned                   0       0
         active                   7       7
         total                    7       7

                                terminals
         un-matched               0       0
         matched but
         different type           0       0
         total                    5       5


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         5               nets
         4               terminals
         2               pmos
         2               nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         5               nets
         4               terminals
         2               pmos
         2               nmos


    Terminal correspondence points
    N1        N0        gnd!
    N3        N6        input
    N2        N2        output
    N4        N1        vdd!

Devices in the netlist but not in the rules:
         pcapacitor
Devices in the rules but not in the netlist:
         cap nfet pfet nmos4 pmos4

The net-lists match.

                               layout  schematic
                                  instances
         un-matched               0       0
         rewired                  0       0
         size errors              0       0
         pruned                   0       0
         active                   4       4
         total                    4       4

                                    nets
         un-matched               0       0
         merged                   0       0
         pruned                   0       0
         active                   5       5
         total                    5       5

                                  terminals
         un-matched               0       0
         matched but
         different type           0       0
         total                    4       4


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         21              nets
         8               terminals
         14              pmos
         14              nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         21              nets
         8               terminals
         14              pmos
         14              nmos


    Terminal correspondence points
    N14       N2        busy
    N13       N1        gnd!
    N19       N7        op_busy
    N18       N10       reset
    N20       N11       start
    N16       N8        state0_en
    N17       N9        state0_loop
    N15       N0        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                                layout  schematic
                                  instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                    28      28
        total                     28      28

                                    nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                    21      21
        total                     21      21

                                  terminals
        un-matched                0       0
        matched but
        different type            0       0
        total                     8       8


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          3199            nets
   12:          31              terminals
   13:          3680            pmos
   14:          3680            nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          3199            nets
   19:          31              terminals
   20:          3680            pmos
   21:          3680            nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N3168     N28       block_en<0>
   26:     N3197     N27       block_en<1>
   27:     N3193     N26       block_en<2>
   28:     N3190     N25       block_en<3>
   29:     N3187     N24       block_en<4>
   30:     N3185     N23       block_en<5>
   31:     N3180     N22       block_en<6>
   32:     N3176     N21       block_en<7>
   33:     N3184     N20       byte_en<0>
   34:     N3179     N19       byte_en<1>
   35:     N3175     N18       byte_en<2>
   36:     N3171     N17       byte_en<3>
   37:     N3172     N0        gnd!
   38:     N3182     N30       r_data<0>
   39:     N3178     N29       r_data<1>
   40:     N3174     N2        r_data<2>
   41:     N3170     N16       r_data<3>
   42:     N3198     N15       r_data<4>
   43:     N3194     N14       r_data<5>
   44:     N3191     N13       r_data<6>
   45:     N3188     N12       r_data<7>
   46:     N3196     N11       rw_en
   47:     N3183     N1        vdd!
   48:     N3195     N10       w_data<0>
   49:     N3192     N9        w_data<1>
   50:     N3189     N8        w_data<2>
   51:     N3186     N7        w_data<3>
   52:     N3181     N6        w_data<4>
   53:     N3177     N5        w_data<5>
   54:     N3173     N4        w_data<6>
   55:     N3169     N3        w_data<7>
   56:
   57: Devices in the netlist but not in the rules:
   58:         pcapacitor
   59: Devices in the rules but not in the netlist:
   60:         cap nfet pfet nmos4 pmos4
   61:
   62: The net-lists match.
   63:
   64:                                  layout  schematic
   65:                                     instances
   66:         un-matched                  0       0
   67:         rewired                     0       0
   68:         size errors                 0       0
   69:         pruned                      0       0
   70:         active                      7360    7360
   71:         total                       7360    7360
   72:
   73:                                       nets
   74:         un-matched                  0       0
   75:         merged                      0       0
   76:         pruned                      0       0
   77:         active                      3199    3199
   78:         total                       3199    3199
   79:
   80:                                     terminals
   81:         un-matched                  0       0
   82:         matched but
   83:         different type              0       0
   84:         total                       31      31
   85:
   86:
   87: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   88:
   89: devbad.out:
   90:
   91: netbad.out:
   92:
   93: mergenet.out:
   94:
   95: termbad.out:
   96:
   97: prunenet.out:
   98:
   99: prunedev.out:
  100:
  101: audit.out:
  102:
  103:
  104: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
  105:
  106: devbad.out:
  107:
  108: netbad.out:
  109:
  110: mergenet.out:
  111:
  112: termbad.out:
  113:
  114: prunenet.out:
  115:
  116: prunedev.out:
  117:
  118: audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          18              nets
   12:          6               terminals
   13:          14              pmos
   14:          14              nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          18              nets
   19:          6               terminals
   20:          14              pmos
   21:          14              nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N16       N8        bit_en
   26:     N12       N0        gnd!
   27:     N13       N2        r_data
   28:     N17       N7        rw_en
   29:     N15       N1        vdd!
   30:     N14       N9        w_data
   31:
   32: Devices in the netlist but not in the rules:
   33:          pcapacitor
   34: Devices in the rules but not in the netlist:
   35:          cap nfet pfet nmos4 pmos4
   36:
   37: The net-lists match.
   38:
   39:                                 layout  schematic
   40:                                    instances
   41:          un-matched                0       0
   42:          rewired                   0       0
   43:          size errors               0       0
   44:          pruned                    0       0
   45:          active                    28      28
   46:          total                     28      28
   47:
   48:                                      nets
   49:          un-matched                0       0
   50:          merged                    0       0
   51:          pruned                    0       0
   52:          active                    18      18
   53:          total                     18      18
   54:
   55:                                    terminals
   56:          un-matched                0       0
   57:          matched but
   58:          different type            0       0
   59:          total                     6       6
   60:
   61:
   62: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   63:
   64: devbad.out:
   65:
   66: netbad.out:
   67:
   68: mergenet.out:
   69:
   70: termbad.out:
   71:
   72: prunenet.out:
   73:
   74: prunedev.out:
   75:
   76: audit.out:
   77:
   78:
   79: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   80:
   81: devbad.out:
   82:
   83: netbad.out:
   84:
   85: mergenet.out:
   86:
   87: termbad.out:
   88:
   89: prunenet.out:
   90:
   91: prunedev.out:
   92:
   93: audit.out:
```

Layout vs Schematic for Cache-Block-Cell
cache_block_cell


```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          420             nets
   12:          24              terminals
   13:          460             pmos
   14:          460             nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          420             nets
   19:          24              terminals
   20:          460             pmos
   21:          460             nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N400      N5        block_en
   26:     N410      N19       byte_en<0>
   27:     N406      N18       byte_en<1>
   28:     N403      N17       byte_en<2>
   29:     N398      N16       byte_en<3>
   30:     N399      N0        gnd!
   31:     N408      N26       r_data<0>
   32:     N405      N25       r_data<1>
   33:     N402      N24       r_data<2>
   34:     N397      N23       r_data<3>
   35:     N419      N22       r_data<4>
   36:     N416      N21       r_data<5>
   37:     N414      N20       r_data<6>
   38:     N412      N15       r_data<7>
   39:     N418      N14       rw_en
   40:     N409      N1        vdd!
   41:     N417      N13       w_data<0>
   42:     N415      N12       w_data<1>
   43:     N413      N11       w_data<2>
   44:     N411      N10       w_data<3>
   45:     N407      N9        w_data<4>
   46:     N404      N8        w_data<5>
   47:     N401      N7        w_data<6>
   48:     N396      N6        w_data<7>
   49:
   50: Devices in the netlist but not in the rules:
   51:         pcapacitor
   52: Devices in the rules but not in the netlist:
   53:         cap nfet pfet nmos4 pmos4
   54:
   55: The net-lists match.
   56:
   57:                               layout  schematic
   58:                                instances
   59:         un-matched            0       0
   60:         rewired               0       0
   61:         size errors           0       0
   62:         pruned                0       0
   63:         active                920     920
   64:         total                 920     920
   65:
   66:                                  nets
   67:         un-matched            0       0
   68:         merged                0       0
   69:         pruned                0       0
   70:         active                420     420
   71:         total                 420     420
   72:
   73:                                terminals
   74:         un-matched            0       0
   75:         matched but
   76:         different type        4       4
   77:         total                 24      24
   78:
   79:
   80: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   81:
   82: devbad.out:
   83:
   84: netbad.out:
   85:
   86: mergenet.out:
   87:
   88: termbad.out:
   89: ? Terminal byte_en<0>'s type in the schematic: input, in the layout: output
   90: ? Terminal byte_en<1>'s type in the schematic: input, in the layout: output
   91: ? Terminal byte_en<2>'s type in the schematic: input, in the layout: output
   92: ? Terminal byte_en<3>'s type in the schematic: input, in the layout: output
   93:
   94: prunenet.out:
   95:
   96: prunedev.out:
   97:
   98: audit.out:
   99:
  100:
  101: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
  102:
  103: devbad.out:
  104:
  105: netbad.out:
  106:
  107: mergenet.out:
  108:
  109: termbad.out:
  110: ? Terminal byte_en<0>'s type in the layout: output, in the schematic: input
  111: ? Terminal byte_en<1>'s type in the layout: output, in the schematic: input
  112: ? Terminal byte_en<2>'s type in the layout: output, in the schematic: input
  113: ? Terminal byte_en<3>'s type in the layout: output, in the schematic: input
  114:
  115: prunenet.out:
  116:
  117: prunedev.out:
  118:
  119: audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
          116             nets
          20              terminals
          112             pmos
          112             nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
          116             nets
          20              terminals
          112             pmos
          112             nmos


    Terminal correspondence points
    N96       N2        byte_en
    N99       N0        gnd!
    N105      N19       r_data<0>
    N103      N18       r_data<1>
    N101      N17       r_data<2>
    N98       N8        r_data<3>
    N115      N7        r_data<4>
    N112      N6        r_data<5>
    N110      N5        r_data<6>
    N108      N4        r_data<7>
    N114      N3        rw_en
    N106      N1        vdd!
    N113      N16       w_data<0>
    N111      N15       w_data<1>
    N109      N14       w_data<2>
    N107      N13       w_data<3>
    N104      N12       w_data<4>
    N102      N11       w_data<5>
    N100      N10       w_data<6>
    N97       N9        w_data<7>

Devices in the netlist but not in the rules:
         pcapacitor
Devices in the rules but not in the netlist:
         cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
         un-matched              0       0
         rewired                 0       0
         size errors             0       0
         pruned                  0       0
         active                  224     224
         total                   224     224

                                   nets
         un-matched              0       0
         merged                  0       0
         pruned                  0       0
         active                  116     116
         total                   116     116

                                 terminals
         un-matched              0       0
         matched but
         different type          0       0
         total                   20      20


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         36              nets
         10              terminals
         28              pmos
         28              nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         36              nets
         10              terminals
         28              pmos
         28              nmos


    Terminal correspondence points
    N28       N16       cache_en
    N33       N10       cache_rw
    N29       N15       cache_tag_rw
    N26       N8        cpu_rw_signal
    N27       N1        gnd!
    N34       N13       read_h_en
    N30       N12       read_m_en
    N31       N0        vdd!
    N35       N14       w_cache
    N32       N11       write_h_en

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                               layout  schematic
                                  instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                   56      56
        total                    56      56

                                    nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                   36      36
        total                    36      36


                                  terminals
        un-matched                0       0
        matched but
        different type            0       0
        total                    10      10


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          75              nets
   12:          13              terminals
   13:          68              pmos
   14:          68              nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          75              nets
   19:          13              terminals
   20:          68              pmos
   21:          68              nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N74       N10       c_rw
   26:     N69       N18       cache0_en
   27:     N64       N19       cache1_en
   28:     N62       N1        gnd!
   29:     N72       N11       hm_signal0
   30:     N71       N12       hm_signal1
   31:     N63       N13       lru_signal
   32:     N73       N14       read_h
   33:     N70       N16       read_m
   34:     N68       N8        state0_en
   35:     N67       N0        vdd!
   36:     N66       N15       write_h
   37:     N65       N17       write_m
   38:
   39: Devices in the netlist but not in the rules:
   40:          pcapacitor
   41: Devices in the rules but not in the netlist:
   42:          cap nfet pfet nmos4 pmos4
   43:
   44: The net-lists match.
   45:
   46:                                 layout  schematic
   47:                                    instances
   48:          un-matched                0       0
   49:          rewired                   0       0
   50:          size errors               0       0
   51:          pruned                    0       0
   52:          active                    136     136
   53:          total                     136     136
   54:
   55:                                      nets
   56:          un-matched                0       0
   57:          merged                    0       0
   58:          pruned                    0       0
   59:          active                    75      75
   60:          total                     75      75
   61:
   62:                                    terminals
   63:          un-matched                0       0
   64:          matched but
   65:          different type            0       0
   66:          total                     13      13
   67:
   68:
   69: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   70:
   71: devbad.out:
   72:
   73: netbad.out:
   74:
   75: mergenet.out:
   76:
   77: termbad.out:
   78:
   79: prunenet.out:
   80:
   81: prunedev.out:
   82:
   83: audit.out:
   84:
   85:
   86: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   87:
   88: devbad.out:
   89:
   90: netbad.out:
   91:
   92: mergenet.out:
   93:
   94: termbad.out:
   95:
   96: prunenet.out:
   97:
   98: prunedev.out:
   99:
  100: audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         8029            nets
         9               terminals
         9164            pmos
         9164            nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         8127            nets
         42              terminals
         9347            pmos
         9347            nmos


    Terminal correspondence points
    N8034     N83       cpu_add<0>
    N8033     N82       cpu_add<1>
    N8032     N56       cpu_add<2>
    N8031     N55       cpu_add<3>
    N8030     N54       cpu_add<4>
    N8029     N53       cpu_add<5>
    N8036     N52       cpu_add<6>
    N8035     N51       cpu_add<7>
    N8037     N93       start

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

    Ill-defined correspondence points.

        N8037   N93  Accepted because one is a subset of the other
        N8037   N93  Accepted because one is a subset of the other


        Device summary for layout
                   bad  total
            pmos     6   9164
            nmos     7   9164


        Device summary for schematic
                   bad  total
            pmos   189   9347
            nmos   190   9347

120 net-list ambiguities were resolved by random selection.


The net-lists failed to match.

                                  layout  schematic
                                     instances
         un-matched                  13      379
         rewired                     132     0
         size errors                 0       0
         pruned                      0       0
         active                      18328   18694
         total                       18328   18694

                                       nets
         un-matched                  157     255
         merged                      0       0
         pruned                      0       0
         active                      8029    8127
         total                       8029    8127

                                     terminals
         un-matched                  1       30
         matched but
         different type              0       0
         total                       9       42


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:
The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFile.
To see the complete information please see the file:
/afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/devbad.out

netbad.out:
The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFile.
To see the complete information please see the file:
/afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netbad.out

mergenet.out:

termbad.out:
The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFile.
To see the complete information please see the file:
/afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/termbad.out

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:
The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFile.
To see the complete information please see the file:
/afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/devbad.out
```

```
  116:
  117: netbad.out:
  118: The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFil
e.
  119: To see the complete information please see the file:
  120: /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netbad.out
  121:
  122: mergenet.out:
  123:
  124: termbad.out:
  125: The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFil
e.
  126: To see the complete information please see the file:
  127: /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/termbad.out
  128:
  129: prunenet.out:
  130:
  131: prunedev.out:
  132:
  133: audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          3760            nets
   12:          50              terminals
   13:          4297            pmos
   14:          4297            nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          3760            nets
   19:          53              terminals
   20:          4297            pmos
   21:          4297            nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N3714     N46       block_en<0>
   26:     N3759     N45       block_en<1>
   27:     N3753     N44       block_en<2>
   28:     N3749     N43       block_en<3>
   29:     N3743     N26       block_en<4>
   30:     N3738     N20       block_en<5>
   31:     N3731     N19       block_en<6>
   32:     N3724     N18       block_en<7>
   33:     N3713     N34       c_data<0>
   34:     N3758     N33       c_data<1>
   35:     N3752     N32       c_data<2>
   36:     N3748     N31       c_data<3>
   37:     N3742     N30       c_data<4>
   38:     N3737     N29       c_data<5>
   39:     N3730     N28       c_data<6>
   40:     N3723     N27       c_data<7>
   41:     N3722     N42       ca_data<0>
   42:     N3716     N41       ca_data<1>
   43:     N3747     N37       ca_data<5>
   44:     N3741     N36       ca_data<6>
   45:     N3734     N35       ca_data<7>
   46:     N3719     N54       cache_en
   47:     N3717     N48       cpu_rw_signal
   48:     N3718     N1        gnd!
   49:     N3728     N57       hm_signal
   50:     N3761     N17       m_data<0>
   51:     N3755     N16       m_data<1>
   52:     N3751     N15       m_data<2>
   53:     N3746     N14       m_data<3>
   54:     N3740     N13       m_data<4>
   55:     N3732     N12       m_data<5>
   56:     N3725     N11       m_data<6>
   57:     N3720     N10       m_data<7>
   58:     N3735     N65       r_data<0>
   59:     N3726     N64       r_data<1>
   60:     N3721     N63       r_data<2>
   61:     N3715     N62       r_data<3>
   62:     N3760     N61       r_data<4>
   63:     N3754     N60       r_data<5>
   64:     N3750     N59       r_data<6>
   65:     N3744     N58       r_data<7>
   66:     N3745     N50       read_h_en
   67:     N3756     N53       read_m
   68:     N3733     N52       read_m_en
   69:     N3757     N47       reset
   70:     N3729     N55       s0
   71:     N3727     N56       s1
   72:     N3736     N0        vdd!
   73:     N3762     N49       w_cache
   74:     N3739     N51       write_h_en
   75:
   76: Devices in the netlist but not in the rules:
   77:         pcapacitor
   78: Devices in the rules but not in the netlist:
   79:         cap nfet pfet nmos4 pmos4
   80:
   81: The net-lists match.
   82:
   83:                                  layout  schematic
   84:                                     instances
   85:         un-matched                  0       0
   86:         rewired                     0       0
   87:         size errors                 0       0
   88:         pruned                      0       0
   89:         active                      8594    8594
   90:         total                       8594    8594
   91:
   92:                                       nets
   93:         un-matched                  0       0
   94:         merged                      0       0
   95:         pruned                      0       0
   96:         active                      3760    3760
   97:         total                       3760    3760
   98:
   99:                                     terminals
  100:         un-matched                  0       0
  101:         matched but
  102:         different type              0       0
  103:         total                       50      53
  104:
  105:
  106: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
  107:
  108: devbad.out:
  109:
  110: netbad.out:
  111:
  112: mergenet.out:
  113:
  114: termbad.out:
  115: ? Terminal ca_data<2> is floating in the schematic.
  116: ? Terminal ca_data<3> is floating in the schematic.
  117: ? Terminal ca_data<4> is floating in the schematic.
  118:
  119: prunenet.out:
```

```
120:
121: prunedev.out:
122:
123: audit.out:
124:
125:
126: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
127:
128: devbad.out:
129:
130: netbad.out:
131:
132: mergenet.out:
133:
134: termbad.out:
135:
136: prunenet.out:
137:
138: prunedev.out:
139:
140: audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         31              nets
         9               terminals
         26              pmos
         26              nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         31              nets
         9               terminals
         26              pmos
         26              nmos


    Terminal correspondence points
    N25       N6        en
    N22       N1        gnd!
    N24       N4        input1
    N23       N5        input2
    N30       N10       output<0>
    N29       N9        output<1>
    N28       N8        output<2>
    N27       N7        output<3>
    N26       N0        vdd!

Devices in the netlist but not in the rules:
         pcapacitor
Devices in the rules but not in the netlist:
         cap nfet pfet nmos4 pmos4

The net-lists match.

                                layout  schematic
                                   instances
         un-matched                0       0
         rewired                   0       0
         size errors               0       0
         pruned                    0       0
         active                    52      52
         total                     52      52

                                     nets
         un-matched                0       0
         merged                    0       0
         pruned                    0       0
         active                    31      31
         total                     31      31

                                   terminals
         un-matched                0       0
         matched but
         different type            0       0
         total                     9       9


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          58              nets
   12:          13              terminals
   13:          53              pmos
   14:          53              nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          58              nets
   19:          13              terminals
   20:          53              pmos
   21:          53              nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N45       N0        gnd!
   26:     N49       N9        input1
   27:     N48       N8        input2
   28:     N46       N2        input3
   29:     N57       N13       output<0>
   30:     N56       N12       output<1>
   31:     N55       N11       output<2>
   32:     N54       N10       output<3>
   33:     N53       N6        output<4>
   34:     N51       N5        output<5>
   35:     N50       N4        output<6>
   36:     N47       N3        output<7>
   37:     N52       N1        vdd!
   38:
   39: Devices in the netlist but not in the rules:
   40:          pcapacitor
   41: Devices in the rules but not in the netlist:
   42:          cap nfet pfet nmos4 pmos4
   43:
   44: The net-lists match.
   45:
   46:                                 layout  schematic
   47:                                    instances
   48:          un-matched                0       0
   49:          rewired                   0       0
   50:          size errors               0       0
   51:          pruned                    0       0
   52:          active                  106     106
   53:          total                   106     106
   54:
   55:                                      nets
   56:          un-matched                0       0
   57:          merged                    0       0
   58:          pruned                    0       0
   59:          active                   58      58
   60:          total                    58      58
   61:
   62:                                    terminals
   63:          un-matched                0       0
   64:          matched but
   65:          different type            0       0
   66:          total                    13      13
   67:
   68:
   69: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   70:
   71: devbad.out:
   72:
   73: netbad.out:
   74:
   75: mergenet.out:
   76:
   77: termbad.out:
   78:
   79: prunenet.out:
   80:
   81: prunedev.out:
   82:
   83: audit.out:
   84:
   85:
   86: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   87:
   88: devbad.out:
   89:
   90: netbad.out:
   91:
   92: mergenet.out:
   93:
   94: termbad.out:
   95:
   96: prunenet.out:
   97:
   98: prunedev.out:
   99:
  100: audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          7               nets
   12:          5               terminals
   13:          3               pmos
   14:          3               nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          7               nets
   19:          5               terminals
   20:          3               pmos
   21:          3               nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N2          N1          gnd!
   26:     N4          N5          input1
   27:     N3          N8          input2
   28:     N5          N3          output
   29:     N6          N0          vdd!
   30:
   31: Devices in the netlist but not in the rules:
   32:          pcapacitor
   33: Devices in the rules but not in the netlist:
   34:          cap nfet pfet nmos4 pmos4
   35:
   36: The net-lists match.
   37:
   38:                                 layout  schematic
   39:                                   instances
   40:          un-matched               0       0
   41:          rewired                  0       0
   42:          size errors              0       0
   43:          pruned                   0       0
   44:          active                   6       6
   45:          total                    6       6
   46:
   47:                                     nets
   48:          un-matched               0       0
   49:          merged                   0       0
   50:          pruned                   0       0
   51:          active                   7       7
   52:          total                    7       7
   53:
   54:                                   terminals
   55:          un-matched               0       0
   56:          matched but
   57:          different type           1       1
   58:          total                    5       5
   59:
   60:
   61: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   62:
   63: devbad.out:
   64:
   65: netbad.out:
   66:
   67: mergenet.out:
   68:
   69: termbad.out:
   70: ? Terminal output's type in the schematic: output, in the layout: input
   71:
   72: prunenet.out:
   73:
   74: prunedev.out:
   75:
   76: audit.out:
   77:
   78:
   79: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   80:
   81: devbad.out:
   82:
   83: netbad.out:
   84:
   85: mergenet.out:
   86:
   87: termbad.out:
   88: ? Terminal output's type in the layout: input, in the schematic: output
   89:
   90: prunenet.out:
   91:
   92: prunedev.out:
   93:
   94: audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         11              nets
         6               terminals
         6               pmos
         6               nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         11              nets
         6               terminals
         6               pmos
         6               nmos


    Terminal correspondence points
    N5        N1        gnd!
    N8        N6        input1
    N7        N5        input2
    N6        N4        input3
    N9        N2        output
    N10       N0        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                                layout  schematic
                                  instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                    12      12
        total                     12      12

                                    nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                    11      11
        total                     11      11

                                  terminals
        un-matched                0       0
        matched but
        different type            0       0
        total                     6       6


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          42              nets
   12:          26              terminals
   13:          24              pmos
   14:          24              nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          42              nets
   19:          26              terminals
   20:          24              pmos
   21:          24              nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N18       N1        gnd!
   26:     N35       N23       input1<0>
   27:     N32       N22       input1<1>
   28:     N29       N21       input1<2>
   29:     N25       N20       input1<3>
   30:     N22       N19       input1<4>
   31:     N19       N18       input1<5>
   32:     N16       N17       input1<6>
   33:     N39       N16       input1<7>
   34:     N24       N24       input2<0>
   35:     N21       N15       input2<1>
   36:     N17       N14       input2<2>
   37:     N40       N13       input2<3>
   38:     N37       N12       input2<4>
   39:     N34       N11       input2<5>
   40:     N31       N10       input2<6>
   41:     N28       N9        input2<7>
   42:     N41       N25       output<0>
   43:     N38       N8        output<1>
   44:     N36       N7        output<2>
   45:     N33       N6        output<3>
   46:     N30       N5        output<4>
   47:     N26       N4        output<5>
   48:     N23       N3        output<6>
   49:     N20       N2        output<7>
   50:     N27       N0        vdd!
   51:
   52: Devices in the netlist but not in the rules:
   53:         pcapacitor
   54: Devices in the rules but not in the netlist:
   55:         cap nfet pfet nmos4 pmos4
   56:
   57: The net-lists match.
   58:
   59:                                 layout  schematic
   60:                                   instances
   61:         un-matched                0       0
   62:         rewired                   0       0
   63:         size errors               0       0
   64:         pruned                    0       0
   65:         active                    48      48
   66:         total                     48      48
   67:
   68:                                     nets
   69:         un-matched                0       0
   70:         merged                    0       0
   71:         pruned                    0       0
   72:         active                    42      42
   73:         total                     42      42
   74:
   75:                                   terminals
   76:         un-matched                0       0
   77:         matched but
   78:         different type            0       0
   79:         total                     26      26
   80:
   81:
   82: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   83:
   84: devbad.out:
   85:
   86: netbad.out:
   87:
   88: mergenet.out:
   89:
   90: termbad.out:
   91:
   92: prunenet.out:
   93:
   94: prunedev.out:
   95:
   96: audit.out:
   97:
   98:
   99: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
  100:
  101: devbad.out:
  102:
  103: netbad.out:
  104:
  105: mergenet.out:
  106:
  107: termbad.out:
  108:
  109: prunenet.out:
  110:
  111: prunedev.out:
  112:
  113: audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         11              nets
         5               terminals
         9               pmos
         9               nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         11              nets
         5               terminals
         9               pmos
         9               nmos


    Terminal correspondence points
    N9        N6        clk
    N7        N8        d
    N6        N0        gnd!
    N10       N9        q
    N8        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                                layout  schematic
                                  instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                    18      18
        total                     18      18

                                    nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                    11      11
        total                     11      11

                                  terminals
        un-matched                0       0
        matched but
        different type            0       0
        total                     5       5

Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         8               nets
         5               terminals
         5               pmos
         5               nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         8               nets
         5               terminals
         5               pmos
         5               nmos


    Terminal correspondence points
    N6        N6        clk
    N4        N2        d
    N3        N0        gnd!
    N7        N3        q
    N5        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                                layout  schematic
                                  instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                    10      10
        total                     10      10

                                    nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                    8       8
        total                     8       8

                                  terminals
        un-matched                0       0
        matched but
        different type            0       0
        total                     5       5

Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         30              nets
         11              terminals
         23              pmos
         23              nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         30              nets
         11              terminals
         23              pmos
         23              nmos


    Terminal correspondence points
    N22       N12       ca_data<0>
    N19       N11       ca_data<1>
    N28       N10       ca_data<2>
    N21       N0        gnd!
    N23       N9        hm_signal
    N27       N8        reset
    N20       N5        tag_valid_data<0>
    N29       N6        tag_valid_data<1>
    N26       N7        tag_valid_data<2>
    N25       N4        tag_valid_data<3>
    N24       N1        vdd!

Devices in the netlist but not in the rules:
         pcapacitor
Devices in the rules but not in the netlist:
         cap nfet pfet nmos4 pmos4

The net-lists match.

                               layout  schematic
                                  instances
         un-matched               0       0
         rewired                  0       0
         size errors              0       0
         pruned                   0       0
         active                   46      46
         total                    46      46

                                    nets
         un-matched               0       0
         merged                   0       0
         pruned                   0       0
         active                   30      30
         total                    30      30

                                  terminals
         un-matched               0       0
         matched but
         different type           0       0
         total                    11      11


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         4               nets
         4               terminals
         1               pmos
         1               nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         4               nets
         4               terminals
         1               pmos
         1               nmos


    Terminal correspondence points
    N0        N0        gnd!
    N2        N3        input
    N1        N5        output
    N3        N1        vdd!

Devices in the netlist but not in the rules:
         pcapacitor
Devices in the rules but not in the netlist:
         cap nfet pfet nmos4 pmos4

The net-lists match.

                               layout  schematic
                                  instances
         un-matched               0       0
         rewired                  0       0
         size errors              0       0
         pruned                   0       0
         active                   2       2
         total                    2       2

                                    nets
         un-matched               0       0
         merged                   0       0
         pruned                   0       0
         active                   4       4
         total                    4       4

                                  terminals
         un-matched               0       0
         matched but
         different type           0       0
         total                    4       4


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          22              nets
   12:          5               terminals
   13:          20              pmos
   14:          20              nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          22              nets
   19:          5               terminals
   20:          20              pmos
   21:          20              nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N17       N0        gnd!
   26:     N18       N9        lru_signal
   27:     N19       N8        read_m_en
   28:     N21       N7        reset
   29:     N20       N1        vdd!
   30:
   31: Devices in the netlist but not in the rules:
   32:          pcapacitor
   33: Devices in the rules but not in the netlist:
   34:          cap nfet pfet nmos4 pmos4
   35:
   36: The net-lists match.
   37:
   38:                                 layout  schematic
   39:                                   instances
   40:          un-matched               0       0
   41:          rewired                  0       0
   42:          size errors              0       0
   43:          pruned                   0       0
   44:          active                   40      40
   45:          total                    40      40
   46:
   47:                                     nets
   48:          un-matched               0       0
   49:          merged                   0       0
   50:          pruned                   0       0
   51:          active                   22      22
   52:          total                    22      22
   53:
   54:                                   terminals
   55:          un-matched               0       0
   56:          matched but
   57:          different type           0       0
   58:          total                    5       5
   59:
   60:
   61: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   62:
   63: devbad.out:
   64:
   65: netbad.out:
   66:
   67: mergenet.out:
   68:
   69: termbad.out:
   70:
   71: prunenet.out:
   72:
   73: prunedev.out:
   74:
   75: audit.out:
   76:
   77:
   78: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   79:
   80: devbad.out:
   81:
   82: netbad.out:
   83:
   84: mergenet.out:
   85:
   86: termbad.out:
   87:
   88: prunenet.out:
   89:
   90: prunedev.out:
   91:
   92: audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         9               nets
         6               terminals
         5               pmos
         5               nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         9               nets
         6               terminals
         5               pmos
         5               nmos


    Terminal correspondence points
    N5        N6        a
    N4        N5        b
    N3        N0        gnd!
    N6        N2        output
    N7        N4        sel
    N8        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                                layout  schematic
                                  instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                    10      10
        total                     10      10

                                    nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                    9       9
        total                     9       9

                                  terminals
        un-matched                0       0
        matched but
        different type            0       0
        total                     6       6


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         51              nets
         27              terminals
         40              pmos
         40              nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         51              nets
         27              terminals
         40              pmos
         40              nmos


    Terminal correspondence points
    N32       N23       a<0>
    N29       N22       a<1>
    N25       N21       a<2>
    N49       N20       a<3>
    N46       N19       a<4>
    N43       N18       a<5>
    N40       N17       a<6>
    N37       N16       a<7>
    N47       N24       b<0>
    N44       N15       b<1>
    N41       N14       b<2>
    N38       N13       b<3>
    N33       N12       b<4>
    N30       N11       b<5>
    N27       N10       b<6>
    N24       N9        b<7>
    N26       N0        gnd!
    N50       N26       output<0>
    N48       N25       output<1>
    N45       N8        output<2>
    N42       N7        output<3>
    N39       N6        output<4>
    N34       N5        output<5>
    N31       N4        output<6>
    N28       N3        output<7>
    N35       N2        sel
    N36       N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                                layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  80      80
        total                   80      80

                                  nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  51      51
        total                   51      51

                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   27      27


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          6               nets
   12:          5               terminals
   13:          2               pmos
   14:          2               nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          6               nets
   19:          5               terminals
   20:          2               pmos
   21:          2               nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N1          N0          gnd!
   26:     N3          N5          input1
   27:     N2          N6          input2
   28:     N4          N2          output
   29:     N5          N1          vdd!
   30:
   31: Devices in the netlist but not in the rules:
   32:          pcapacitor
   33: Devices in the rules but not in the netlist:
   34:          cap nfet pfet nmos4 pmos4
   35:
   36: The net-lists match.
   37:
   38:                                 layout  schematic
   39:                                   instances
   40:          un-matched               0       0
   41:          rewired                  0       0
   42:          size errors              0       0
   43:          pruned                   0       0
   44:          active                   4       4
   45:          total                    4       4
   46:
   47:                                     nets
   48:          un-matched               0       0
   49:          merged                   0       0
   50:          pruned                   0       0
   51:          active                   6       6
   52:          total                    6       6
   53:
   54:                                   terminals
   55:          un-matched               0       0
   56:          matched but
   57:          different type           0       0
   58:          total                    5       5
   59:
   60:
   61: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   62:
   63: devbad.out:
   64:
   65: netbad.out:
   66:
   67: mergenet.out:
   68:
   69: termbad.out:
   70:
   71: prunenet.out:
   72:
   73: prunedev.out:
   74:
   75: audit.out:
   76:
   77:
   78: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   79:
   80: devbad.out:
   81:
   82: netbad.out:
   83:
   84: mergenet.out:
   85:
   86: termbad.out:
   87:
   88: prunenet.out:
   89:
   90: prunedev.out:
   91:
   92: audit.out:
```

Layout vs Schematic for NOR3

nor3


```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          9               nets
   12:          6               terminals
   13:          4               pmos
   14:          4               nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          9               nets
   19:          6               terminals
   20:          4               pmos
   21:          4               nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N3          N0          gnd!
   26:     N6          N6          input1
   27:     N5          N5          input2
   28:     N4          N4          input3
   29:     N7          N2          output
   30:     N8          N1          vdd!
   31:
   32: Devices in the netlist but not in the rules:
   33:          pcapacitor
   34: Devices in the rules but not in the netlist:
   35:          cap nfet pfet nmos4 pmos4
   36:
   37: The net-lists match.
   38:
   39:                                 layout  schematic
   40:                                    instances
   41:          un-matched                0       0
   42:          rewired                   0       0
   43:          size errors               0       0
   44:          pruned                    0       0
   45:          active                    8       8
   46:          total                     8       8
   47:
   48:                                      nets
   49:          un-matched                0       0
   50:          merged                    0       0
   51:          pruned                    0       0
   52:          active                    9       9
   53:          total                     9       9
   54:
   55:                                    terminals
   56:          un-matched                0       0
   57:          matched but
   58:          different type            0       0
   59:          total                     6       6
   60:
   61:
   62: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   63:
   64: devbad.out:
   65:
   66: netbad.out:
   67:
   68: mergenet.out:
   69:
   70: termbad.out:
   71:
   72: prunenet.out:
   73:
   74: prunedev.out:
   75:
   76: audit.out:
   77:
   78:
   79: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   80:
   81: devbad.out:
   82:
   83: netbad.out:
   84:
   85: mergenet.out:
   86:
   87: termbad.out:
   88:
   89: prunenet.out:
   90:
   91: prunedev.out:
   92:
   93: audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          67              nets
   12:          19              terminals
   13:          72              pmos
   14:          72              nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          67              nets
   19:          19              terminals
   20:          72              pmos
   21:          72              nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N58       N2        clk
   26:     N65       N16       d<0>
   27:     N63       N15       d<1>
   28:     N61       N14       d<2>
   29:     N59       N13       d<3>
   30:     N56       N12       d<4>
   31:     N53       N11       d<5>
   32:     N52       N10       d<6>
   33:     N50       N9        d<7>
   34:     N49       N0        gnd!
   35:     N51       N18       q<0>
   36:     N48       N17       q<1>
   37:     N66       N8        q<2>
   38:     N64       N7        q<3>
   39:     N62       N6        q<4>
   40:     N60       N5        q<5>
   41:     N57       N4        q<6>
   42:     N54       N3        q<7>
   43:     N55       N1        vdd!
   44:
   45: Devices in the netlist but not in the rules:
   46:          pcapacitor
   47: Devices in the rules but not in the netlist:
   48:          cap nfet pfet nmos4 pmos4
   49:
   50: The net-lists match.
   51:
   52:                                 layout  schematic
   53:                                    instances
   54:          un-matched                0       0
   55:          rewired                   0       0
   56:          size errors               0       0
   57:          pruned                    0       0
   58:          active                  144     144
   59:          total                   144     144
   60:
   61:                                      nets
   62:          un-matched                0       0
   63:          merged                    0       0
   64:          pruned                    0       0
   65:          active                   67      67
   66:          total                    67      67
   67:
   68:                                    terminals
   69:          un-matched                0       0
   70:          matched but
   71:          different type            0       0
   72:          total                    19      19
   73:
   74:
   75: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   76:
   77: devbad.out:
   78:
   79: netbad.out:
   80:
   81: mergenet.out:
   82:
   83: termbad.out:
   84:
   85: prunenet.out:
   86:
   87: prunedev.out:
   88:
   89: audit.out:
   90:
   91:
   92: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   93:
   94: devbad.out:
   95:
   96: netbad.out:
   97:
   98: mergenet.out:
   99:
  100: termbad.out:
  101:
  102: prunenet.out:
  103:
  104: prunedev.out:
  105:
  106: audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          36              nets
   12:          11              terminals
   13:          26              pmos
   14:          26              nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          36              nets
   19:          13              terminals
   20:          26              pmos
   21:          26              nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N26       N16       input<0>
   26:     N25       N15       input<1>
   27:     N34       N14       input<2>
   28:     N33       N2        input<3>
   29:     N32       N3        input<4>
   30:     N31       N4        input<5>
   31:     N30       N5        input<6>
   32:     N29       N6        input<7>
   33:     N28       N13       s0
   34:     N27       N7        s1
   35:     N35       N8        w_cache
   36:
   37: Devices in the netlist but not in the rules:
   38:          pcapacitor
   39: Devices in the rules but not in the netlist:
   40:          cap nfet pfet nmos4 pmos4
   41:
   42: The net-lists match.
   43:
   44:                                 layout  schematic
   45:                                    instances
   46:          un-matched                0       0
   47:          rewired                   0       0
   48:          size errors               0       0
   49:          pruned                    0       0
   50:          active                   52      52
   51:          total                    52      52
   52:
   53:                                      nets
   54:          un-matched                0       0
   55:          merged                    0       0
   56:          pruned                    0       0
   57:          active                   36      36
   58:          total                    36      36
   59:
   60:                                   terminals
   61:          un-matched                0       0
   62:          matched but
   63:          different type            0       0
   64:          total                    11      13
   65:
   66:
   67: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   68:
   69: devbad.out:
   70:
   71: netbad.out:
   72:
   73: mergenet.out:
   74:
   75: termbad.out:
   76:
   77: prunenet.out:
   78:
   79: prunedev.out:
   80:
   81: audit.out:
   82:
   83:
   84: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   85:
   86: devbad.out:
   87:
   88: netbad.out:
   89:
   90: mergenet.out:
   91:
   92: termbad.out:
   93:
   94: prunenet.out:
   95:
   96: prunedev.out:
   97:
   98: audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          308             nets
   12:          25              terminals
   13:          349             pmos
   14:          349             nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          308             nets
   19:          25              terminals
   20:          349             pmos
   21:          349             nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N296      N7        clk
   26:     N306      N75       data_receive<0>
   27:     N301      N74       data_receive<1>
   28:     N300      N73       data_receive<2>
   29:     N297      N72       data_receive<3>
   30:     N294      N71       data_receive<4>
   31:     N290      N70       data_receive<5>
   32:     N286      N69       data_receive<6>
   33:     N284      N68       data_receive<7>
   34:     N283      N0        gnd!
   35:     N288      N65       memory_en
   36:     N305      N67       op_busy
   37:     N289      N66       read_en
   38:     N304      N57       read_h
   39:     N298      N62       read_h_en
   40:     N302      N56       read_m
   41:     N291      N64       read_m_en
   42:     N303      N2        reset
   43:     N307      N55       start
   44:     N293      N60       state0_en
   45:     N299      N61       state0_loop
   46:     N292      N1        vdd!
   47:     N287      N59       write_h
   48:     N295      N63       write_h_en
   49:     N285      N58       write_m
   50:
   51: Devices in the netlist but not in the rules:
   52:          pcapacitor
   53: Devices in the rules but not in the netlist:
   54:          cap nfet pfet nmos4 pmos4
   55:
   56: The net-lists match.
   57:
   58:                                  layout  schematic
   59:                                     instances
   60:          un-matched                 0       0
   61:          rewired                    0       0
   62:          size errors                0       0
   63:          pruned                     0       0
   64:          active                     698     698
   65:          total                      698     698
   66:
   67:                                       nets
   68:          un-matched                 0       0
   69:          merged                     0       0
   70:          pruned                     0       0
   71:          active                     308     308
   72:          total                      308     308
   73:
   74:                                     terminals
   75:          un-matched                 0       0
   76:          matched but
   77:          different type             0       0
   78:          total                      25      25
   79:
   80:
   81: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   82:
   83: devbad.out:
   84:
   85: netbad.out:
   86:
   87: mergenet.out:
   88:
   89: termbad.out:
   90:
   91: prunenet.out:
   92:
   93: prunedev.out:
   94:
   95: audit.out:
   96:
   97:
   98: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   99:
  100: devbad.out:
  101:
  102: netbad.out:
  103:
  104: mergenet.out:
  105:
  106: termbad.out:
  107:
  108: prunenet.out:
  109:
  110: prunedev.out:
  111:
  112: audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         441             nets
         19              terminals
         487             pmos
         487             nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         441             nets
         19              terminals
         487             pmos
         487             nmos


    Terminal correspondence points
    N422      N26       block_en<0>
    N439      N25       block_en<1>
    N435      N24       block_en<2>
    N432      N23       block_en<3>
    N430      N22       block_en<4>
    N429      N21       block_en<5>
    N426      N4        block_en<6>
    N425      N3        block_en<7>
    N436      N19       ca_reg<0>
    N433      N18       ca_reg<1>
    N431      N17       ca_reg<2>
    N427      N16       cache_tag_rw
    N424      N0        gnd!
    N438      N15       reset
    N423      N13       tag_valid_data<0>
    N440      N20       tag_valid_data<1>
    N437      N9        tag_valid_data<2>
    N434      N14       tag_valid_data<3>
    N428      N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   974     974
        total                    974     974

                                   nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   441     441
        total                    441     441

                                 terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    19      19


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

Layout vs Schematic for Tag/Valid Block-unit cell

tag_valid_block_cell


```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          60              nets
   12:          12              terminals
   13:          56              pmos
   14:          56              nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          60              nets
   19:          12              terminals
   20:          56              pmos
   21:          56              nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N48       N3        byte_en
   26:     N50       N0        gnd!
   27:     N53       N8        r_data<0>
   28:     N52       N7        r_data<1>
   29:     N51       N6        r_data<2>
   30:     N49       N5        r_data<3>
   31:     N59       N2        rw_en
   32:     N54       N1        vdd!
   33:     N58       N11       w_data<0>
   34:     N57       N10       w_data<1>
   35:     N56       N9        w_data<2>
   36:     N55       N4        w_data<3>
   37:
   38: Devices in the netlist but not in the rules:
   39:         pcapacitor
   40: Devices in the rules but not in the netlist:
   41:         cap nfet pfet nmos4 pmos4
   42:
   43: The net-lists match.
   44:
   45:                                layout  schematic
   46:                                  instances
   47:         un-matched               0       0
   48:         rewired                  0       0
   49:         size errors              0       0
   50:         pruned                   0       0
   51:         active                   112     112
   52:         total                    112     112
   53:
   54:                                    nets
   55:         un-matched               0       0
   56:         merged                   0       0
   57:         pruned                   0       0
   58:         active                   60      60
   59:         total                    60      60
   60:
   61:                                  terminals
   62:         un-matched               0       0
   63:         matched but
   64:         different type           0       0
   65:         total                    12      12
   66:
   67:
   68: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   69:
   70: devbad.out:
   71:
   72: netbad.out:
   73:
   74: mergenet.out:
   75:
   76: termbad.out:
   77:
   78: prunenet.out:
   79:
   80: prunedev.out:
   81:
   82: audit.out:
   83:
   84:
   85: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   86:
   87: devbad.out:
   88:
   89: netbad.out:
   90:
   91: mergenet.out:
   92:
   93: termbad.out:
   94:
   95: prunenet.out:
   96:
   97: prunedev.out:
   98:
   99: audit.out:
```

```
    1: @(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
    2:
    3: Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.
edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Pro
ject/LVS/schematic
    4: Like matching is enabled.
    5: Net swapping is enabled.
    6: Using terminal names as correspondence points.
    7: Compiling Diva LVS rules...
    8:
    9:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layo
ut/netlist
   10:         count
   11:          6               nets
   12:          5               terminals
   13:          2               pmos
   14:          2               nmos
   15:
   16:     Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/sche
matic/netlist
   17:         count
   18:          6               nets
   19:          5               terminals
   20:          2               pmos
   21:          2               nmos
   22:
   23:
   24:     Terminal correspondence points
   25:     N4          N4          en
   26:     N1          N0          gnd!
   27:     N3          N5          input
   28:     N2          N2          output
   29:     N5          N1          vdd!
   30:
   31: Devices in the netlist but not in the rules:
   32:          pcapacitor
   33: Devices in the rules but not in the netlist:
   34:          cap nfet pfet nmos4 pmos4
   35:
   36: The net-lists match.
   37:
   38:                                 layout  schematic
   39:                                   instances
   40:          un-matched               0       0
   41:          rewired                  0       0
   42:          size errors              0       0
   43:          pruned                   0       0
   44:          active                   4       4
   45:          total                    4       4
   46:
   47:                                     nets
   48:          un-matched               0       0
   49:          merged                   0       0
   50:          pruned                   0       0
   51:          active                   6       6
   52:          total                    6       6
   53:
   54:                                   terminals
   55:          un-matched               0       0
   56:          matched but
   57:          different type           0       0
   58:          total                    5       5
   59:
   60:
   61: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
   62:
   63: devbad.out:
   64:
   65: netbad.out:
   66:
   67: mergenet.out:
   68:
   69: termbad.out:
   70:
   71: prunenet.out:
   72:
   73: prunedev.out:
   74:
   75: audit.out:
   76:
   77:
   78: Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout
   79:
   80: devbad.out:
   81:
   82: netbad.out:
   83:
   84: mergenet.out:
   85:
   86: termbad.out:
   87:
   88: prunenet.out:
   89:
   90: prunedev.out:
   91:
   92: audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         27              nets
         19              terminals
         16              pmos
         16              nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         27              nets
         19              terminals
         16              pmos
         16              nmos


    Terminal correspondence points
    N15       N2        en
    N9        N0        gnd!
    N11       N16       input<0>
    N8        N15       input<1>
    N25       N14       input<2>
    N23       N13       input<3>
    N21       N12       input<4>
    N19       N11       input<5>
    N17       N10       input<6>
    N13       N9        input<7>
    N26       N18       output<0>
    N24       N17       output<1>
    N22       N8        output<2>
    N20       N7        output<3>
    N18       N6        output<4>
    N14       N5        output<5>
    N12       N4        output<6>
    N10       N3        output<7>
    N16       N1        vdd!

Devices in the netlist but not in the rules:
         pcapacitor
Devices in the rules but not in the netlist:
         cap nfet pfet nmos4 pmos4

The net-lists match.

                               layout  schematic
                                  instances
         un-matched               0       0
         rewired                  0       0
         size errors              0       0
         pruned                   0       0
         active                   32      32
         total                    32      32

                                    nets
         un-matched               0       0
         merged                   0       0
         pruned                   0       0
         active                   27      27
         total                    27      27

                                  terminals
         un-matched               0       0
         matched but
         different type           0       0
         total                    19      19


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         6               nets
         4               terminals
         1               pmos
         1               nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         6               nets
         6               terminals
         1               pmos
         1               nmos


    Terminal correspondence points
    N3        N6        input
    N2        N2        output
    N5        N3        sel
    N4        N5        selnot

Devices in the netlist but not in the rules:
         pcapacitor
Devices in the rules but not in the netlist:
         cap nfet pfet nmos4 pmos4

The net-lists match.

                               layout  schematic
                                  instances
         un-matched               0       0
         rewired                  0       0
         size errors              0       0
         pruned                   0       0
         active                   2       2
         total                    2       2

                                    nets
         un-matched               0       0
         merged                   0       0
         pruned                   0       0
         active                   6       6
         total                    6       6

                                  terminals
         un-matched               0       0
         matched but
         different type           0       0
         total                    4       6


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         8               nets
         5               terminals
         5               pmos
         5               nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         8               nets
         5               terminals
         5               pmos
         5               nmos


    Terminal correspondence points
    N3        N0        gnd!
    N5        N5        input1
    N4        N4        input2
    N6        N2        output
    N7        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                                layout  schematic
                                  instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                    10      10
        total                     10      10

                                    nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                    8       8
        total                     8       8

                                  terminals
        un-matched                0       0
        matched but
        different type            0       0
        total                     5       5


Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /afs/umbc.edu/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS -l -s -t /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout/netlist
        count
         7               nets
         5               terminals
         4               pmos
         4               nmos

    Net-list summary for /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic/netlist
        count
         7               nets
         5               terminals
         4               pmos
         4               nmos


    Terminal correspondence points
    N2        N0        gnd!
    N4        N6        input1
    N3        N4        input2
    N5        N2        output
    N6        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                                layout  schematic
                                  instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                    8       8
        total                     8       8

                                    nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                    7       7
        total                     7       7

                                terminals
        un-matched                0       0
        matched but
        different type            0       0
        total                     5       5

Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /afs/umbc.edu/users/m/g/mgalib1/home/Project/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```