Md Mehedi Hassan Galib

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Professional Summary

- 12+ years of experience in EDA/Silicon development tools, including Cadence, Synopsys, and Mentor Graphics.
- 12+ years of experience in programming languages, including Matlab, Python, C, and C++.
- 10+ years of experience in HDL languages, including Verilog, System Verilog, and System C.
- 10+ years of experience in designing low-power, energy-efficient systems, with a focus on optimizing the trade-offs between performance, power, and area.
- 10+ years of experience in both full custom and semi-custom ASIC design flow, covering all stages from RTL to GDSII.
- 5+ years of experience with machine learning tools running on CPU, GPU, and Raspberry Pi; specifically targeting resource-constrained edge devices.
- 4+ years of experience in neuromorphic computing, spike neural networks, and Hebbian learning.
- 3+ years of experience and knowledge in computer architecture concepts, including microprocessor architecture, memory systems, on-chip interconnection networks, and hardware/software partitioning.
- Results-oriented, self-motivated, and proactive, with demonstrated creative and critical thinking capabilities.
- Skilled in technical writing; write, understand and follow standard operating procedures (SOPs).
- Experienced in collaborating and leading in a team environment.

Technical Skills

- **EDA/CAD tools** : Cadence Spectre, Cadence Virtuoso, Cadence SoC Encounter, Cadence Innovus, Mentor Graphics Calibre, Synopsys Fusion Compiler, Synopsys VCS, Synopsys Design Compiler, Synopsys ICC II, Synopsys Prime-time, Synopsys Prime-power, Synopsys Platform Architect.
- **FPGA platform** : Xilinx Vitis HLS, Xilinx Vivado, Altera Quartus, Altera Modelsim, NIOS.
- **Machine learning tools** : Pytorch, TensorFlow, Scikit-learn, Keras, Pandas, Matplotlib, CUDA, HPC(MPI).
- **Languages** : Python, C, C++, Assembly language, NodeJS, R.
- **Script** : Perl, TCL, Eldo, HSpice, PSpice, Make, Linux OS, Shell(bash).
- **HDL** : Verilog, System Verilog, VHDL, System C.
- **Debugging tool** : ELVIS board, Oscilloscope, Logic Analyzer, UVM.
- **Microcontroller** : Raspberry Pi, Arduino, Atmel(8051, AVR32), Microchip(pic16, pic32) .
- **Software** : Matlab, MPLab, Proteus, Windmil, HP Labs-CACTI Cache Architectural Simulator.
- **Application** : MS office, MS Word, MS Excel, MS PowerPoint, MS Visio, Latex, Figma, Canva.
- **Version control** : GitHub, SVN, BitBucket.
- **Web programming** : HTML, CSS, JavaScript, React.
- **Soft skill** : Leadership, Adaptability, Communication, Goal-Oriented, Problem-Solving, Technical Writing.

Work Experience

Meta Platforms, Inc. **WA, USA**

ASIC/FPGA Hardware Engineer Intern for an AR/VR Project at Reality Labs. *Summer 2024*

- Developed a Laser Controller (LC) for LCoS using FPGA/ASIC technology. The LC was used to synchronize the laser pulses with the LCoS signal, generating true-color RGB images through a compact micro-display.
  - Designed and developed RTL or HLS code for various IPs; participated in micro-architecture, design, and verification reviews, providing feedback; analyzed designs to enhance SWaP-C (size, weight, power, cost); supported and developed verification infrastructure; improved verification coverage; and supported simulation accelerators and post-silicon validation.

Lasarrus Clinic and Research Center **MD, USA**

FPGA & ASIC Engineer Intern *Fall 2023-Present*

- Implemented an FPGA-based prototype of the WearME device for COPD patients.
  - Designed and developed RTL code for the FPGA fabric and C/C++ code for the ARM processor of the Altera SoC DE10-nano to maintain SW-HW co-design. Performed simulations in Quartus Prime; designed ADC/DAC interfaces for peripheral sensors integration; reduced EMI and ESI; designed PLL for peripheral input; implemented deep learning algorithms; managed data visualization; designed PCBs and performed soldering; debugged using a logic analyzer and oscilloscope; and handled documentation and risk management in accordance with FDA requirements.

Intel Corporation **MA, USA**

Xeon SoC Structural Design Intern *Summer 2022 - Spring 2023*

- Next generation Xeon Processor design
  - Designed high-speed SoC clock distribution with optimized skew, conducted static timing analysis, jitter simulation, ANOVA simulation, power analysis, and global variation analysis. Additionally, managed latency issues and utilized Intel internal clock builder tools with Synopsys Fusion Compiler and ICC II for back-end ASIC design flow.

Computer Engineering Department, University of Maryland Baltimore County **MD, USA**

Graduate Assistant *Spring 2021 - Present*

- **Teaching Assistant**
  - Advanced Computer Architecture, Advanced Machine Learning, Digital Image Processing, Programmable Logic Devices, Principles of Electronic Circuits, Introductory Circuit Theory.
- **Research Assistant**
  - Cross-medium communication project: Utilized the BINDNET PyTorch framework to build a machine-learning-based modulation scheme for multipath communication featuring edge devices. Funded by NSF and accepted at a top IEEE conference.)
  - Bio-inspired spectral-temporal architecture for Cognitive Radio: Conducted review and simulation using Matlab, and prepared the manuscript. Accepted in a top IEEE Transaction.)
  - Dynamic partial reconfiguration of Xilinx FPGA boards (Zed, Zybo, Artix-7), layout design of various flip-flops using 14nm FinFET technology, and High-Level Synthesis (HLS) implementation of a spike neural network. Funded by ONR and accepted in both an IEEE Transaction and an IEEE conference.

Electrical and Electronic Engineering in Islamic University of Technology **Gazipur, Bangladesh**
Assistant Professor *Fall 2016 - Winter 2021*

- Theory Courses : Semiconductor Devices, Advanced Electronics I, Numerical Methods.
- Lab Courses: VLSI Circuits Lab, Numerical Methods Lab, Simulation Lab, Digital Electronics Lab, Advanced Electronics I Lab, Peripherals & Microprocessor Based Design Lab, Signal & System Lab, AC Circuit Lab.

CSA & VLSI lab of Kyung Hee University **Suwon, South Korea**
Graduate Research Assistant *Spring 2013 - Fall 2015*

- Total Ionization Dose (TID) Effect on Cache Memory (SRAM) using a tape-out chip with 28nm FD SOI technology.
  - Conducted literature review, performed simulations, designed layouts, developed low power system designs, and verified chips under radiation conditions.
- Radiation Effect in Combinational Circuit using a tape-out chip with 28nm FD SOI technology.
  - Designed radiation-hardened flip-flops, single event transient-tolerant buffers, and ring oscillators.
- Robust Flip-Flop Design to Mitigate Single Event Upset using tape-out chip with 130nm HCOMS9SOI technology.
  - Conducted literature review, performed simulations using Eldo, designed layouts, and verified chips.

Computer Science and Engineering in Ahsanullah University of Science and Technology **Dhaka, Bangladesh**
Lecturer *Winter 2012 - Spring 2013*

- Lab Courses: Digital System Design Lab.

Education

- **Ph.D. Candidate in Computer Engineering** Spring 2021 - Present
  University of Maryland Baltimore County, USA, CGPA: 3.97/4.00. Transcript, Proposal.
- **MSc. in Computer Engineering** Spring 2021 - Spring 2023
  University of Maryland Baltimore County, USA, CGPA: 3.97/4.00 . Transcript, Dissertation.
- **MSc. in Electronics and Radio Engineering** Spring 2013 - Fall 2015
  Kyung Hee University, South Korea, CGPA: 4.10/4.30. Transcript, Dissertation.
- **BSc. in Electrical and Electronic Engineering** Spring 2008 - Fall 2012
  Islamic University of Technology, Dhaka, Bangladesh, CGPA: 3.98/4.00. Transcript, Dissertation.

Project, Training, Workshop

- **Course capstone project**
  - "FPGA Realization of an Spike Neural Network Model for Opportunistic Spectrum Access."(Report)
  - "Human Physical Activity Recognition Using Stacked Long Short-Term Memory."(Report)
  - "Analysis and Comparison of Methods for Learning Correlations in the Breast Cancer Wisconsin (Diagnostic) Dataset."(Report)
  - "Temporal Signature Detection Among Different Motor Tasks Using Neuromorphic Computing."(Report)
  - "Analysis of Branch Prediction Strategies."(Report)
  - "Application of Machine Learning in EDA Tool Flow." (Report)
  - "Comparison of Deep Neural Network Implementations in FPGA and ASIC." (Report)
  - "Demonstration of a Center-Out Reaching Task Using Virtual Reality, Implemented with VR Builder-Simulink."(Report)
  - "64 byte cache design using VHDL and layout design using $0.6\mu m$ planer technology." (Report)
  - "Hardware-software co-design for the Gaussian Naive Bayes method using SystemC and SystemVerilog." (Report)
  - Multi-Cycle Microprocessor without Interlocked Pipeline Stages, developed using Samsung's 180 nm PDK.
- **Volunteer project, Training & Workshop**
  - Microcontroller-Based Power Factor (PF) Meter using PIC 16F877.
  - Mortality Rate Analysis for a Local Insurance Company, utilizing MS Access for database querying.
  - Six months training on Programmable Logic Controller (PLC), organized by System Engineering Limited. (Certificate)
  - Short course on "Third Generation FACTS Devices: Dynamic Modeling and Simulation." (Certificate)

Publication

- List of Publication: (Please click the link.)

Extra Curriculum Courses

- Machine Learning, Deep Learning Specialization, Python for Everybody Specialization, Python 3 Programming, Excel Skills for Business Specialization, Google IT Automation with Python Professional Certificate.